

## N-Channel 650V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	650	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.95
$Q_g$ (Max.) (nC)	15	
$Q_{gs}$ (nC)	3	
$Q_{gd}$ (nC)	6	
Configuration	Single	

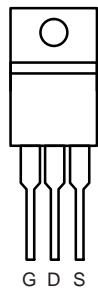
### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC



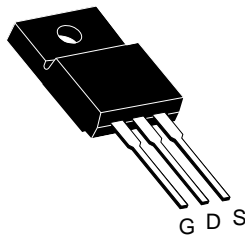
**RoHS\***  
COMPLIANT

TO-220AB



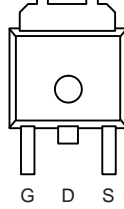
Top View

TO-220 FULLPAK



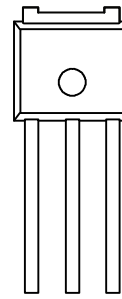
Top View

TO-252

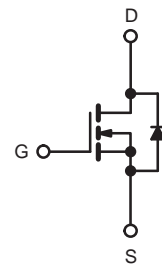


Top View

TO-251



Top View




N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	650	V
Gate-Source Voltage		$V_{GS}$	$\pm 30$	
Continuous Drain Current <sup>e</sup>	$V_{GS}$ at 10 V	$I_D$	$T_C = 25$ °C	A
Continuous Drain Current			$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	16	
Linear Derating Factor			1.67/0.8/0.3	W/°C
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	120	mJ
Repetitive Avalanche Current <sup>a</sup>		$I_{AR}$	34	A
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	17	mJ
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	205/35/30	W
Peak Diode Recovery $dV/dt^c$		$dV/dt$	4.5	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		300	
Mounting Torque	6-32 or M3 screw		10	
			1.1	N · m

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25$  °C,  $L = 24$  mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 3.2$  A (see fig. 12).
- $I_{SD} \leq 3.2$  A,  $dI/dt \leq 90$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.
- Drain current limited by maximum junction temperature.

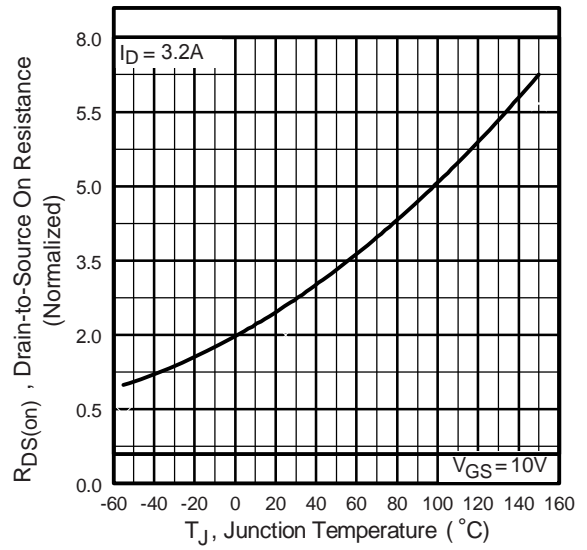
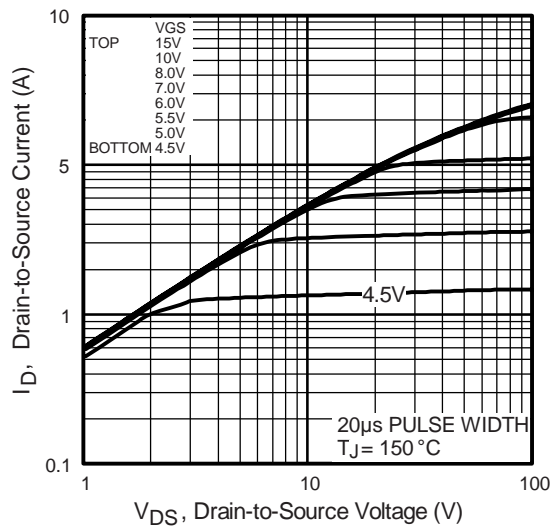
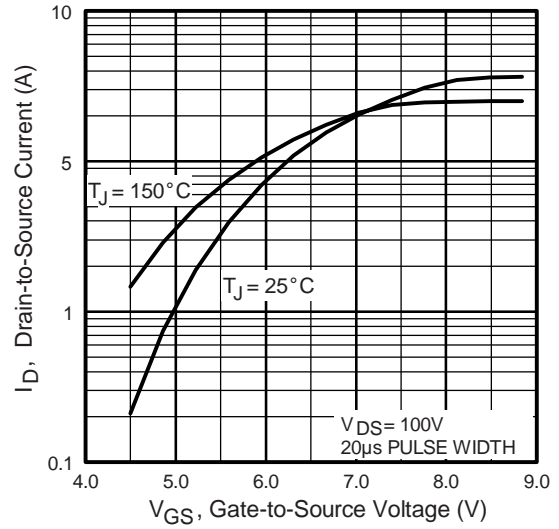
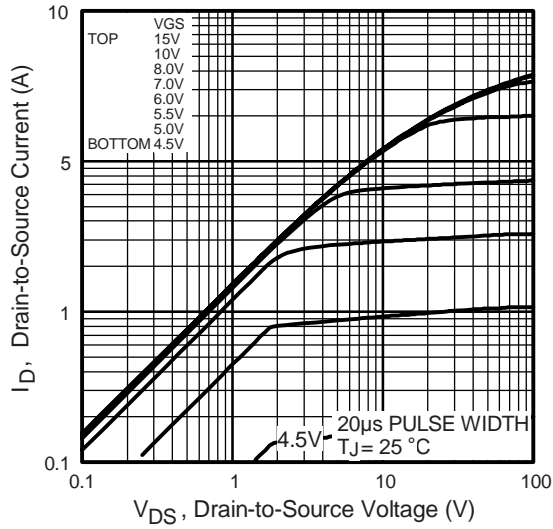
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.6/1.2/0.6	

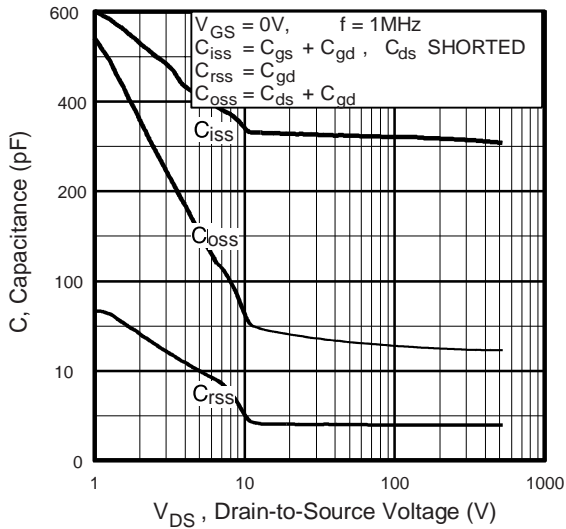
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^d$	-	0.6	-	mV/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$   $I_D = 2.5\text{ A}^b$	-	0.95	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 2.5\text{ A}$	8	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	320	-	pF
Output Capacitance	$C_{oss}$		-	75	-	
Reverse Transfer Capacitance	$C_{rss}$		-	4	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	500	-
			$V_{DS} = 520\text{ V}, f = 1.0\text{ MHz}$	-	83	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 520\text{ V}^c$	-	14	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$   $I_D = 2.5\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	15	nC
Gate-Source Charge	$Q_{gs}$		-	-	3	
Gate-Drain Charge	$Q_{gd}$		-	-	6	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 325\text{ V}, I_D = 3.2\text{ A}$ $R_G = 9.1\text{ }\Omega, R_D = 62\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	18	-	ns
Rise Time	$t_r$		-	40	-	
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	
Fall Time	$t_f$		-	30	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	16	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 3.2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 3.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	180	-	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	2.1	3.2	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

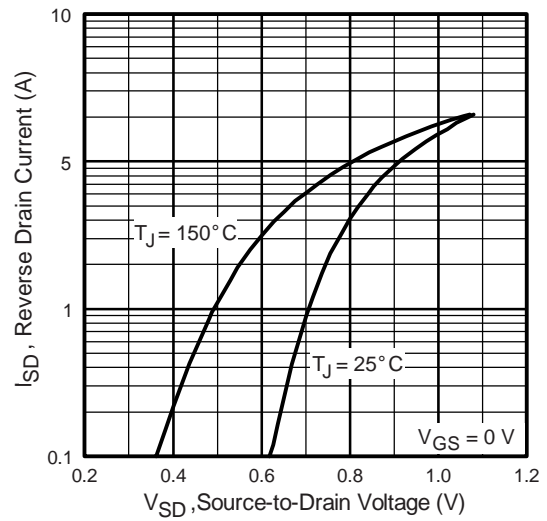
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .
- $t = 60\text{ s}, f = 60\text{ Hz}$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

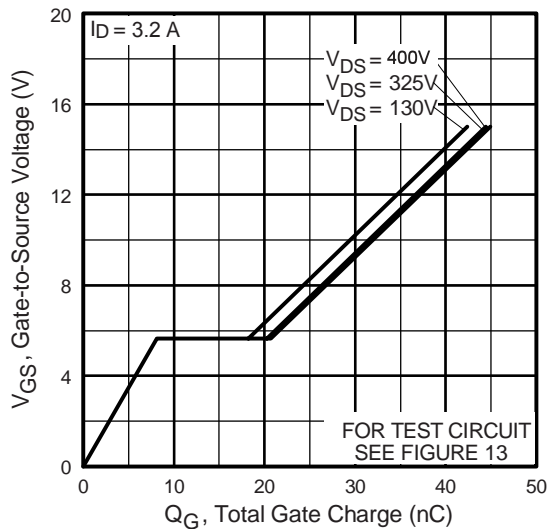




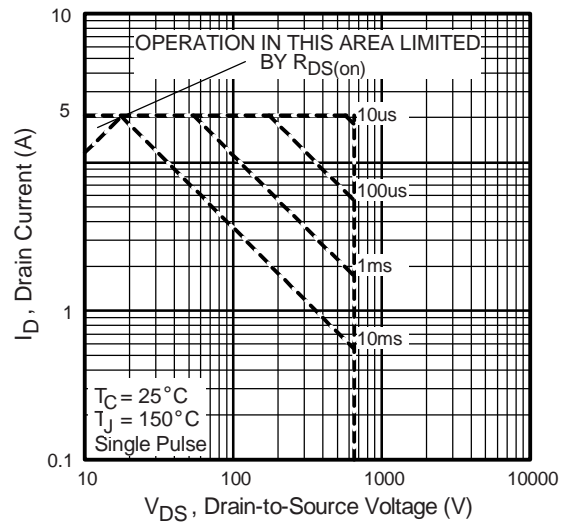
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



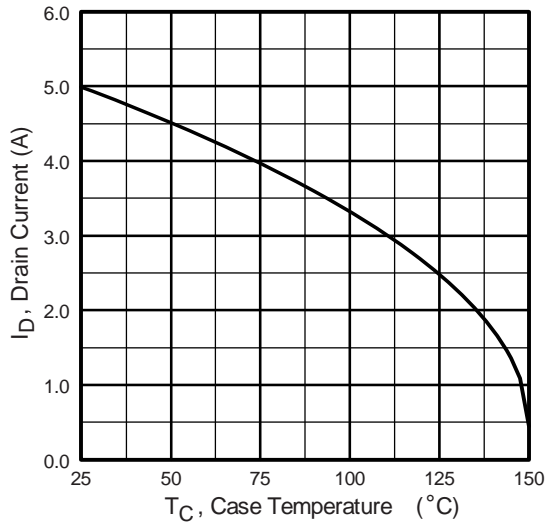
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



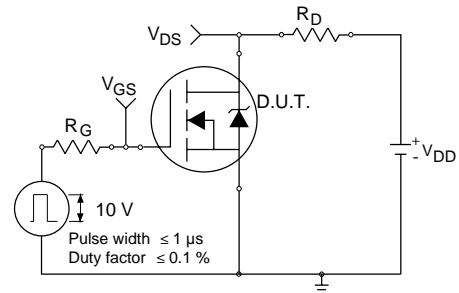
**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



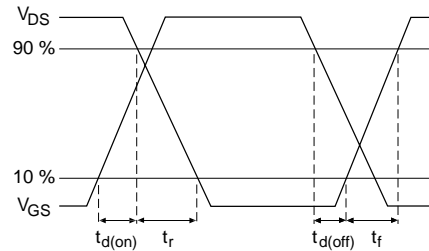
**Fig. 8 - Maximum Safe Operating Area**



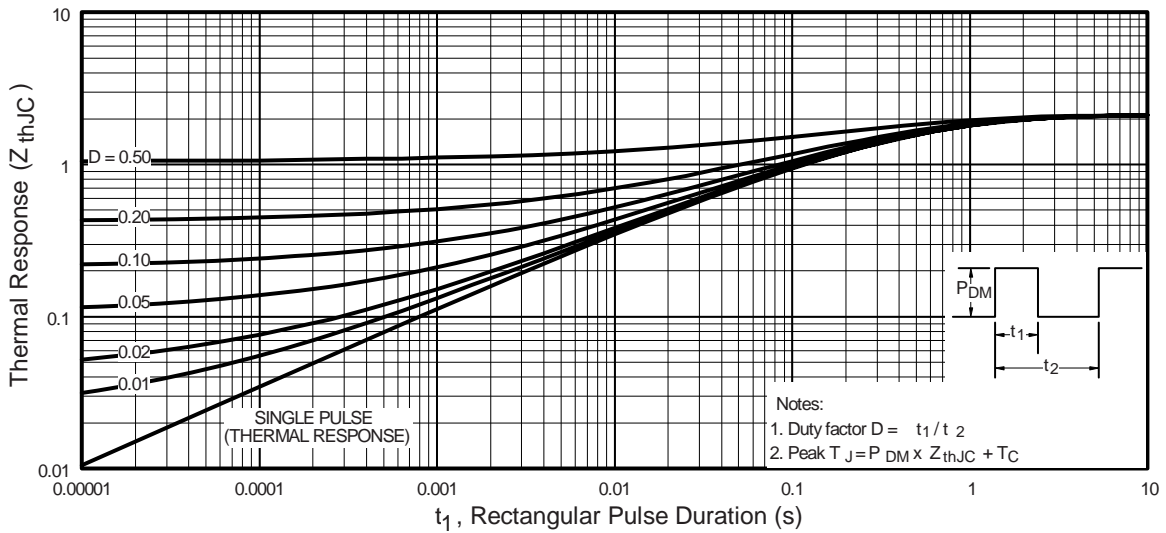
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



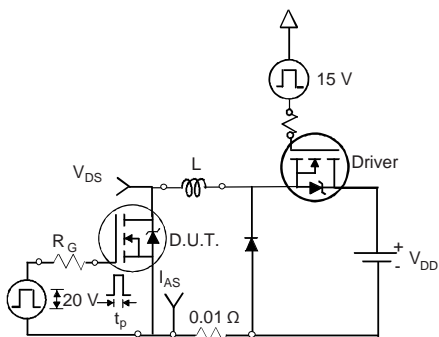
**Fig. 10a - Switching Time Test Circuit**



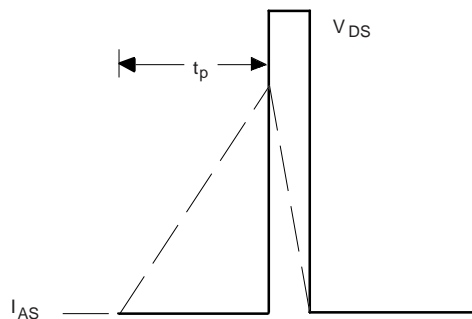
**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**

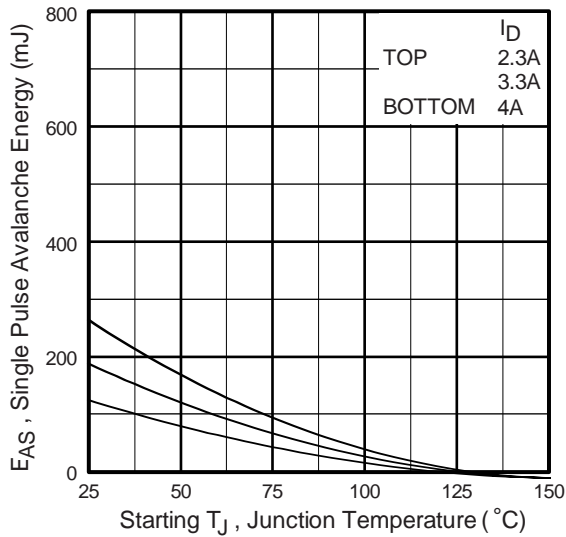


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

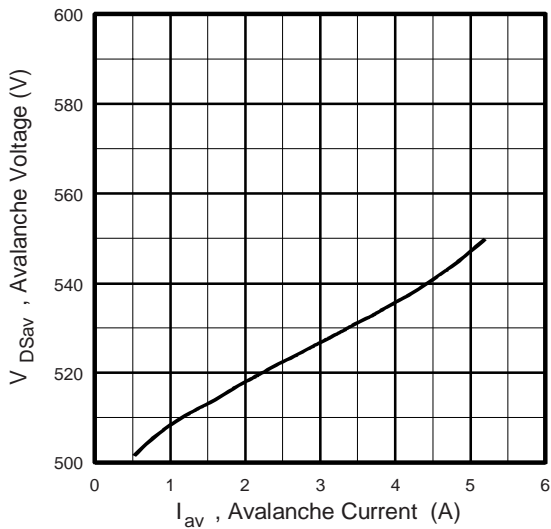


Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current

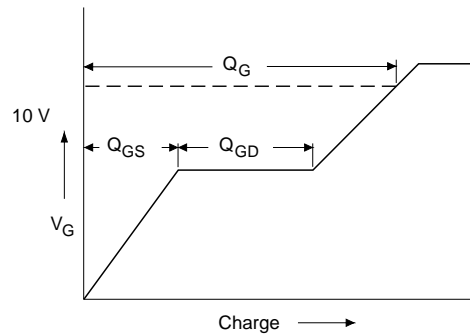


Fig. 13a - Basic Gate Charge Waveform

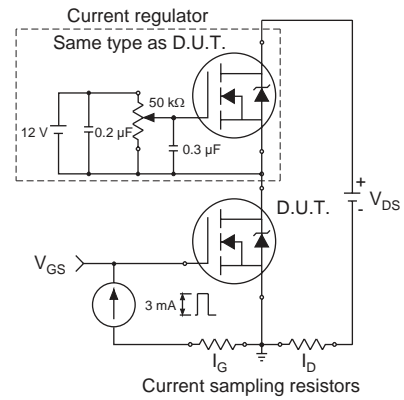
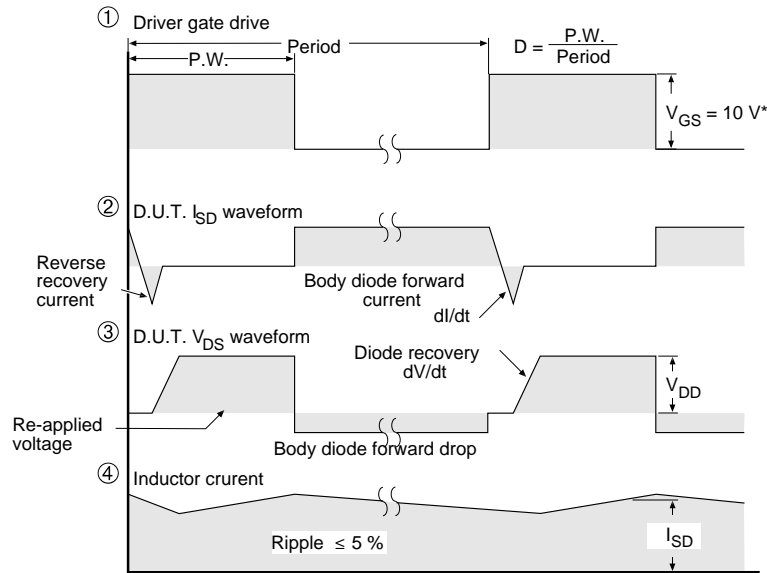
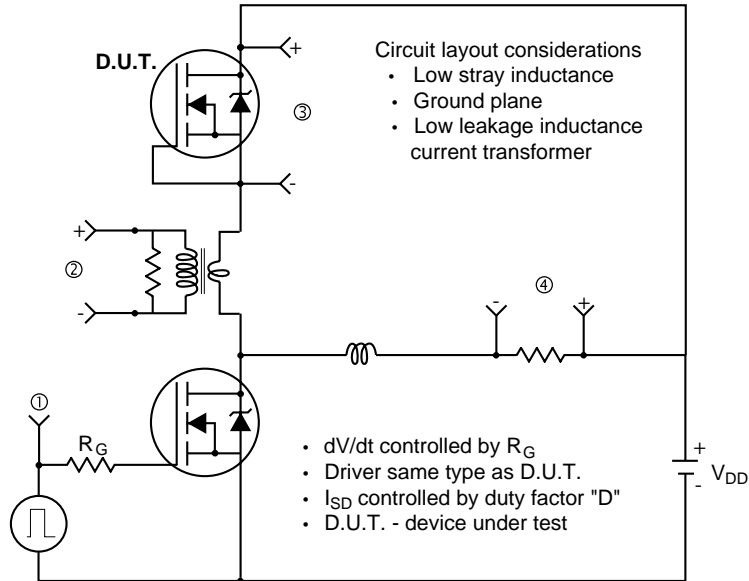


Fig. 13b - Gate Charge Test Circuit

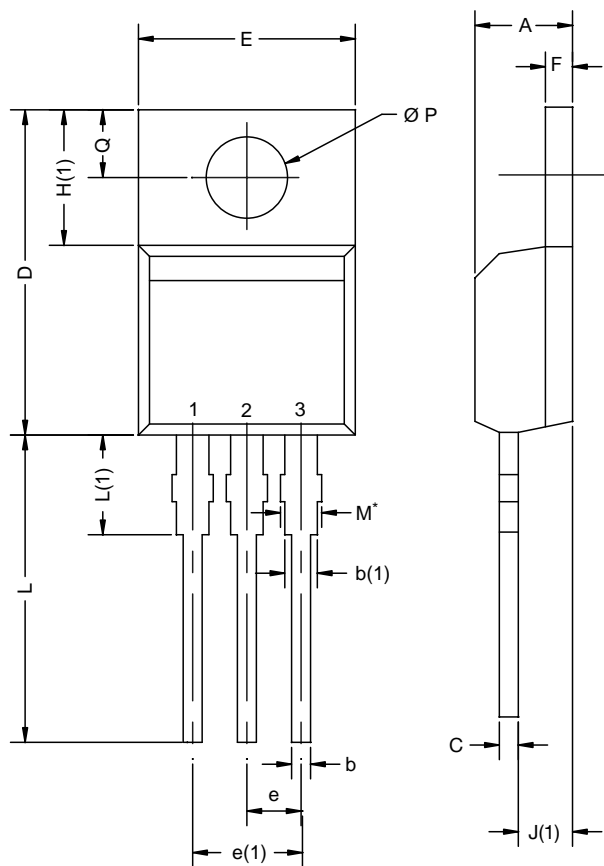
**Peak Diode Recovery dV/dt Test Circuit**



\*  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

### TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

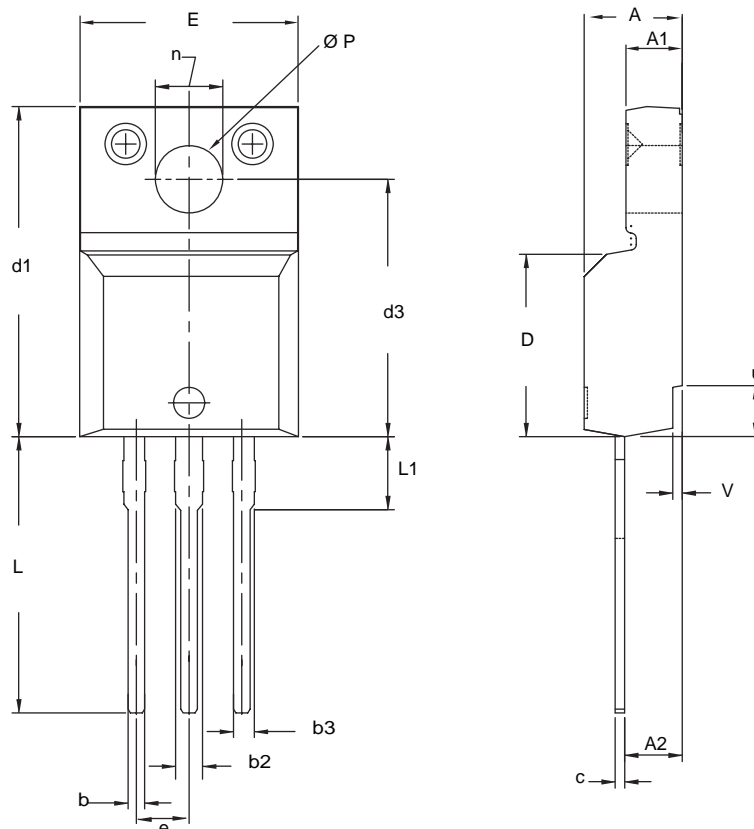
ECN: X12-0208-Rev. N, 08-Oct-12  
DWG: 5471

**Notes**

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM



**TO-220 FULLPAK (HIGH VOLTAGE)**



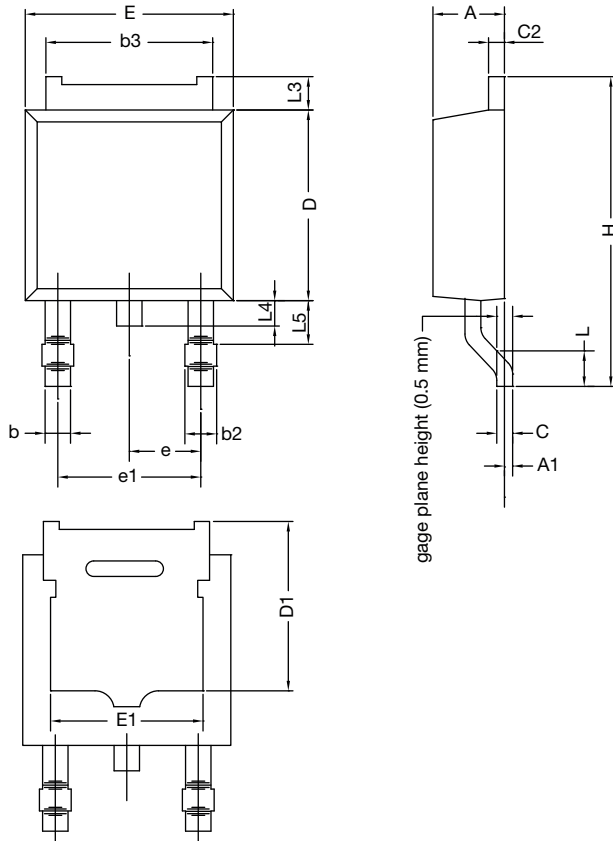
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
$\varnothing P$	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
DWG: 5972

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

**TO-252AA CASE OUTLINE**

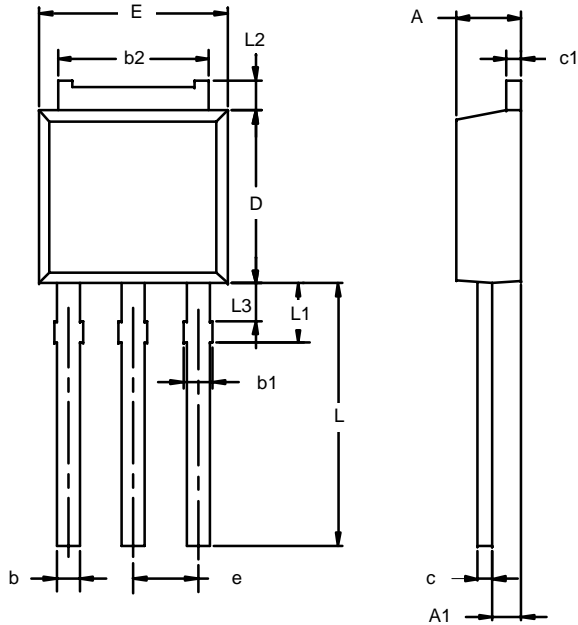


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

**Note**

- Dimension L3 is for reference only.

**TO-251AA (DPAK)**



Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	2.21	2.38	0.087	0.094
<b>A1</b>	0.89	1.14	0.035	0.045
<b>b</b>	0.71	0.89	0.028	0.035
<b>b1</b>	0.76	1.14	0.030	0.045
<b>b2</b>	5.23	5.43	0.206	0.214
<b>c</b>	0.46	0.58	0.018	0.023
<b>c1</b>	0.46	0.58	0.018	0.023
<b>D</b>	5.97	6.22	0.235	0.245
<b>E</b>	6.48	6.73	0.255	0.265
<b>e</b>	2.28 BSC		0.090 BSC	
<b>L</b>	8.89	9.53	0.350	0.375
<b>L1</b>	1.91	2.28	0.075	0.090
<b>L2</b>	0.89	1.27	0.035	0.050
<b>L3</b>	1.15	1.52	0.045	0.060
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5346				

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