

N-Channel 55 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)
55	0.0052 at V _{GS} = 10 V	100	79

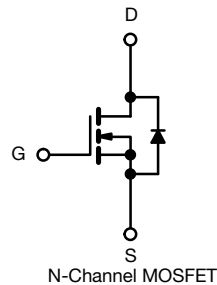
FEATURES

- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- Power Supply
 - Secondary Synchronous Rectification
- DC/DC Converter



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	55	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	100 ^d
		T _C = 70 °C	80 ^d
Pulsed Drain Current	I _{DM}	300	A
Avalanche Current	I _{AS}	50	
Single Avalanche Energy ^a	E _{AS}	170	mJ
Maximum Power Dissipation ^a	P _D	T _C = 25 °C	125 ^b
		T _A = 25 °C ^c	3.0
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W
Junction-to-Case (Drain)	R _{thJC}	1	

Notes:

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).
- Package limited.

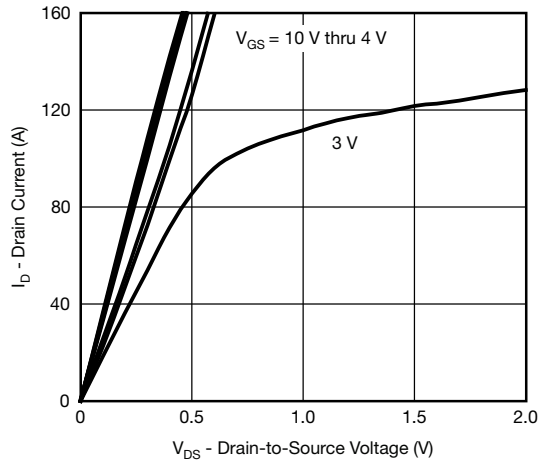
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	55			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 55\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 55\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 55\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 22\text{ A}$		0.0052	0.0058	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		159		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$		3286		pF
Output Capacitance	C_{oss}			705		
Reverse Transfer Capacitance	C_{rss}			283		
Total Gate Charge ^c	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		87	131	nC
Gate-Source Charge ^c	Q_{gs}			15.3		
Gate-Drain Charge ^c	Q_{gd}			12.2		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.5	2.7	5.4	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		11	20	ns
Rise Time ^c	t_r			7	14	
Turn-Off Delay Time ^c	$t_{d(off)}$			45	68	
Fall Time ^c	t_f			7	14	
Drain-Source Body Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}$ ^b						
Continuous Current	I_S				90	A
Pulsed Current	I_{SM}				300	
Forward Voltage ^a	V_{SD}	$F = 10\text{ A}, V_{GS} = 0\text{ V}$		0.72	1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		42	63	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			2.5	3.8	A
Reverse Recovery Charge	Q_{rr}				52	78

Notes:

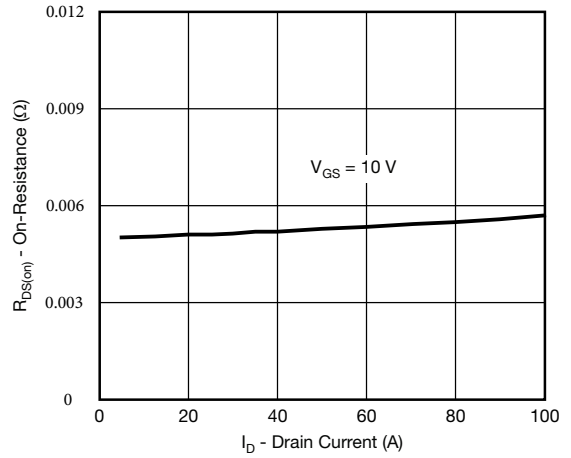
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

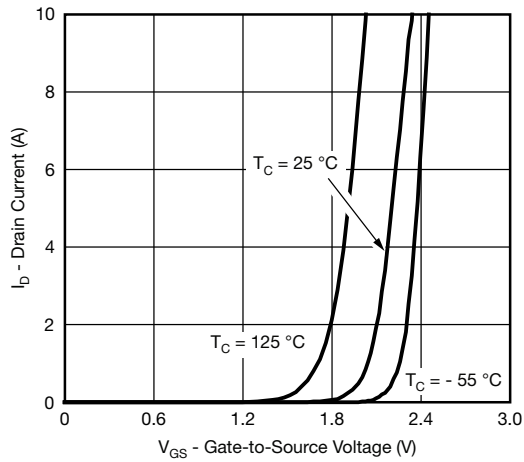
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



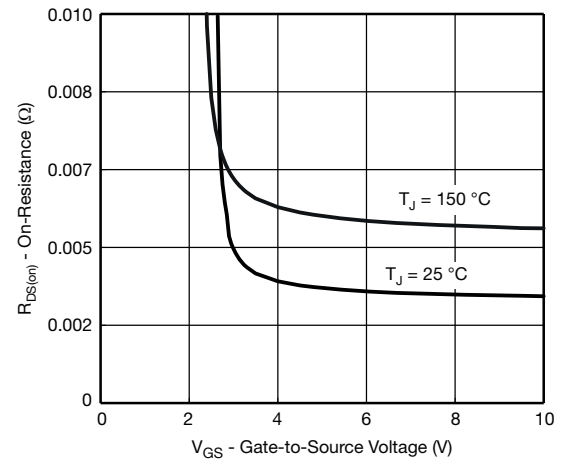
Output Characteristics



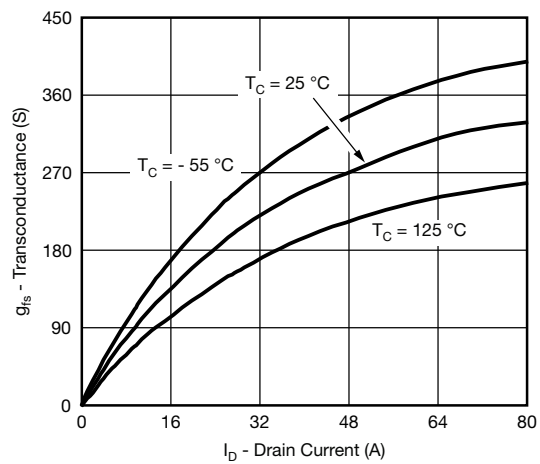
On-Resistance vs. Drain Current



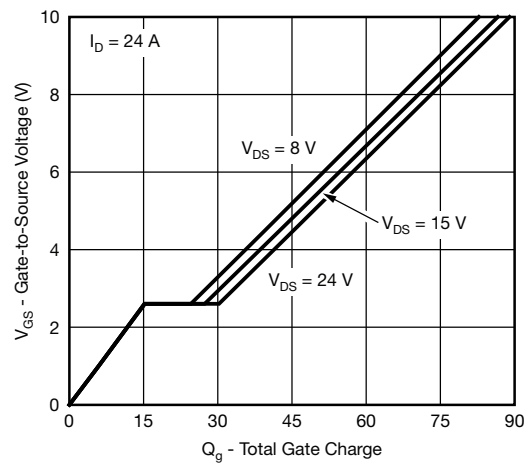
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage

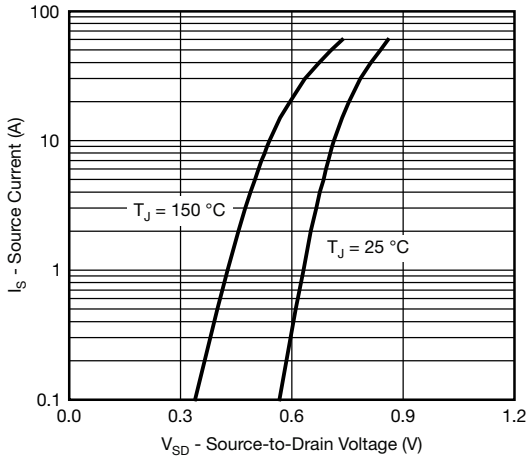


Transconductance

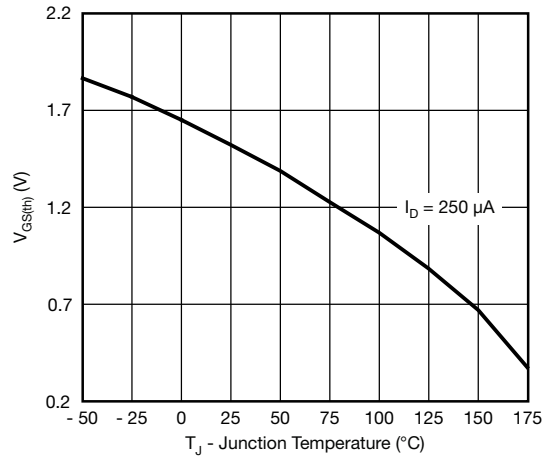


Gate Charge

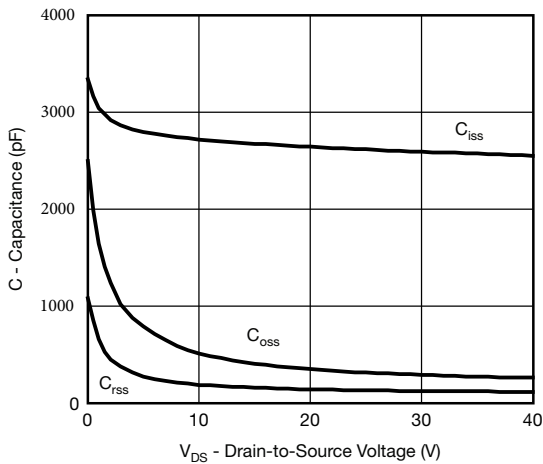
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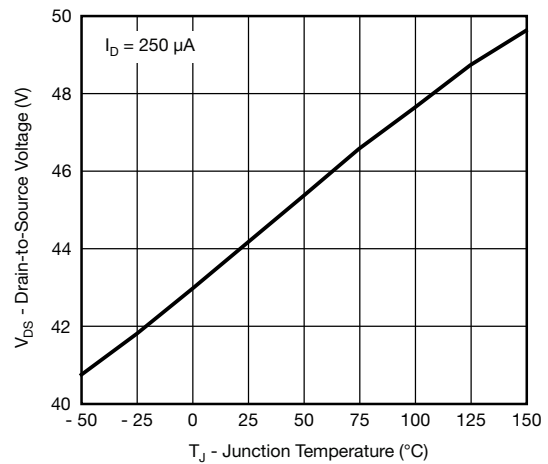
Source-Drain Diode Forward Voltage



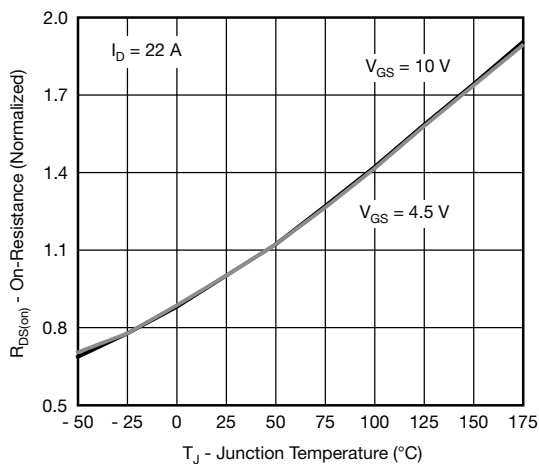
Threshold Voltage



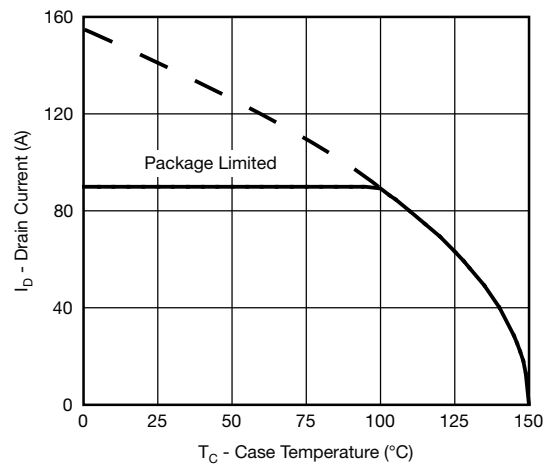
Capacitance



Drain Source Breakdown vs. Junction Temperature

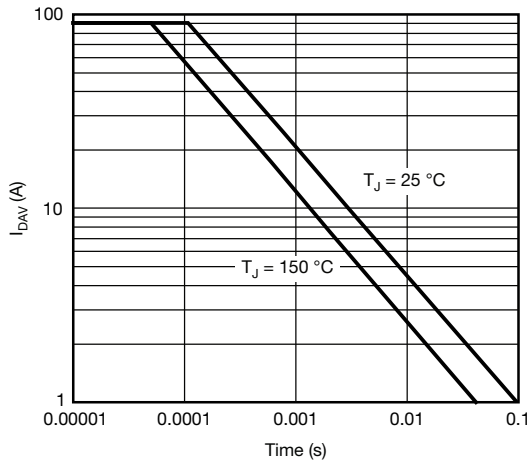


On-Resistance vs. Junction Temperature

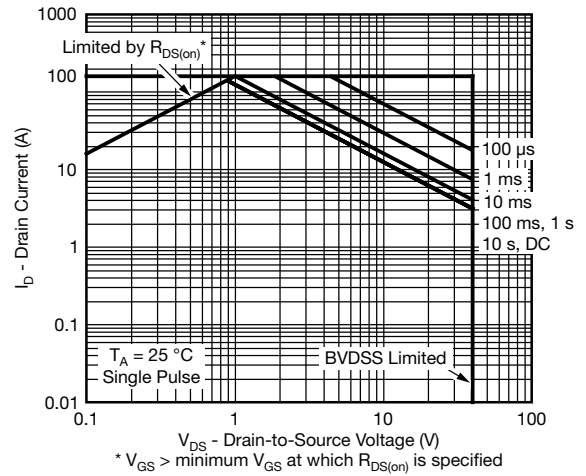


Current Derating

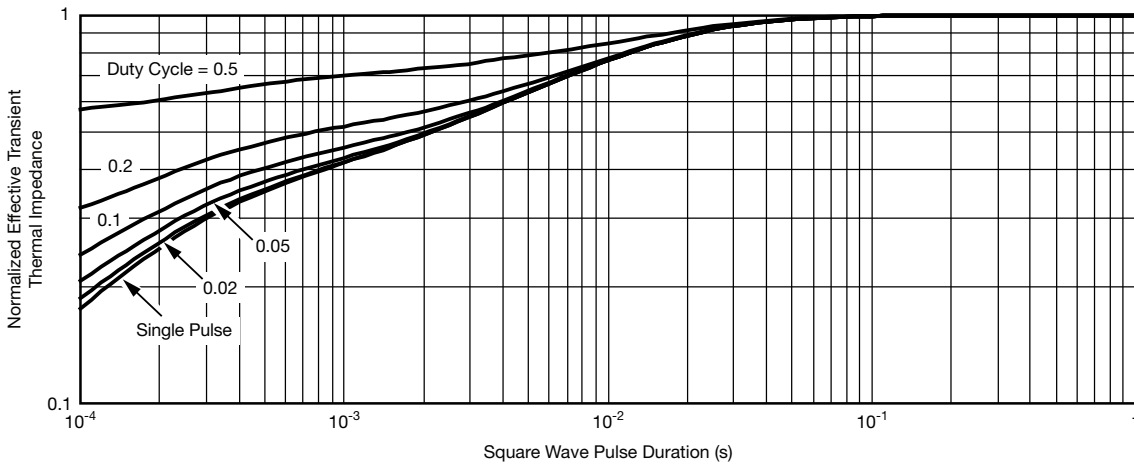
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Single Pulse Avalanche Current Capability vs. Time

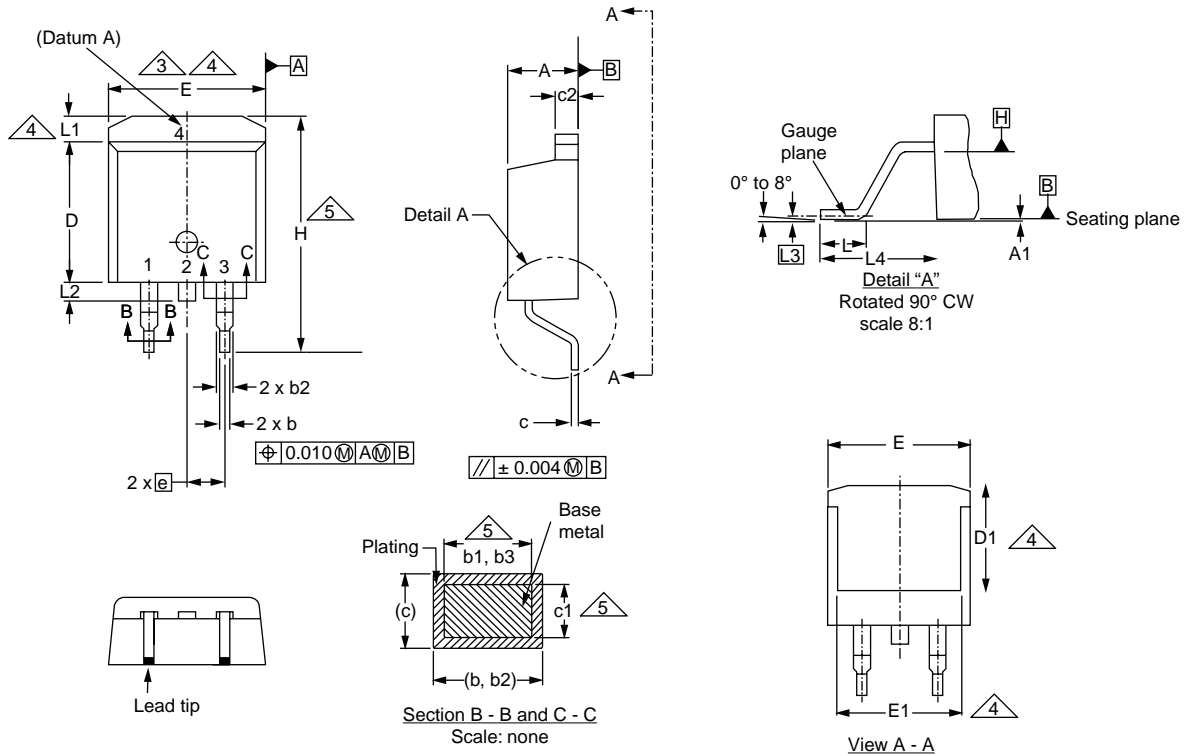


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

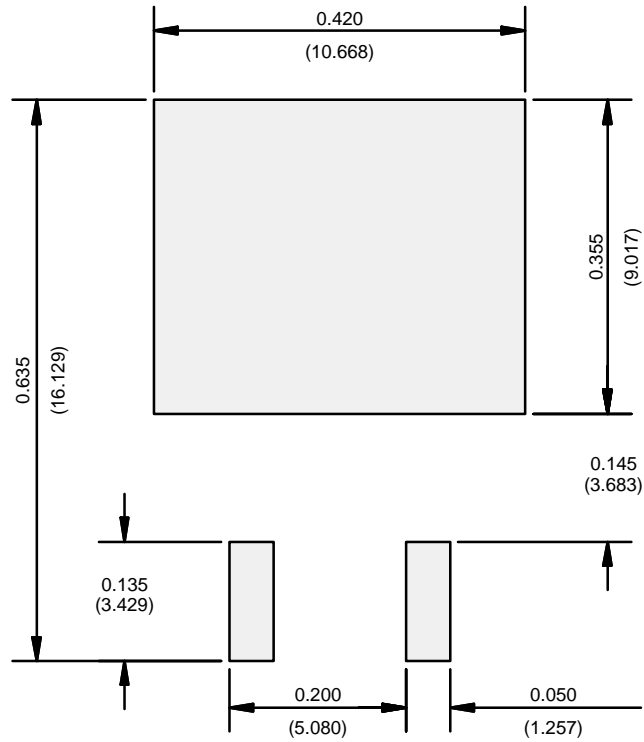
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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