

N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ.)
30	0.0014 at V _{GS} = 10 V	65	75 nC
	0.0017 at V _{GS} = 4.5 V	50	

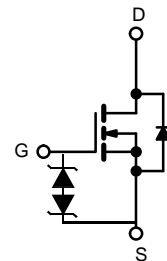
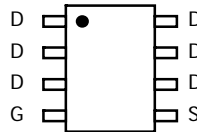
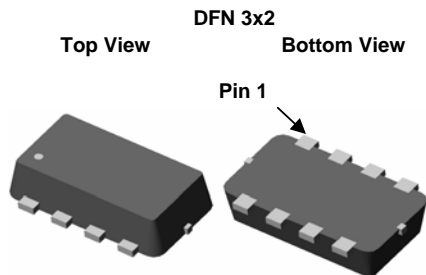
FEATURES

- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested
- Typical ESD protection



APPLICATIONS

- Notebook PC Core
- VRM/POL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 175 °C)	I _D	T _C = 25 °C	65 ^{a, e}
		T _C = 70 °C	54 ^e
		T _A = 25 °C	33 ^{b, c}
		T _A = 70 °C	28.8 ^{b, c}
Pulsed Drain Current	I _{DM}	260	A
Avalanche Current Pulse	I _{AS}	63	
Single Pulse Avalanche Energy	E _{AS}	110	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	65 ^{a, e}
		T _A = 25 °C	35 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	89
		T _C = 70 °C	56
		T _A = 25 °C	7.65 ^{b, c}
		T _A = 70 °C	4.85 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	15	20	°C/W
Maximum Junction-to-Case	R _{thJC}	1.1	1.5	

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 90 °C/W.
- Calculated based on maximum junction temperature.

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

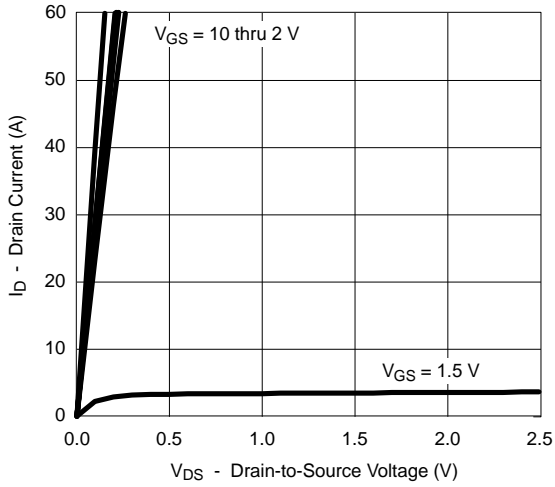
Parameter	Symbol	Test Conditions	Min .	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.5		1.4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	70			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		0.0014	0.0020	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		0.0017	0.0022	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 24\text{ V}, I_D = 10\text{ A}$		100		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3859		pF
Output Capacitance	C_{oss}			996		
Reverse Transfer Capacitance	C_{rss}			300		
Total Gate Charge	Q_g	$V_{DS} = 24\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		75		nC
		$V_{DS} = 24\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		63.5		
Gate-Source Charge	Q_{gs}	$V_{DS} = 24\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		35		
Gate-Drain Charge	Q_{gd}			30		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 24\text{ V}, R_L = 0.555\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		18	27	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 24\text{ V}, R_L = 0.625\text{ }\Omega$ $I_D \cong 8\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		55	83	
Rise Time	t_r			180	270	
Turn-Off Delay Time	$t_{d(off)}$			55	83	
Fall Time	t_f			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			65	A
Pulse Diode Forward Current ^a	I_{SM}				260	
Body Diode Voltage	V_{SD}	$I_S = 8\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		52	78	ns
Body Diode Reverse Recovery Charge	Q_{rr}			70.2	105	nC
Reverse Recovery Fall Time	t_a			27		ns
Reverse Recovery Rise Time	t_b			25		

Notes:

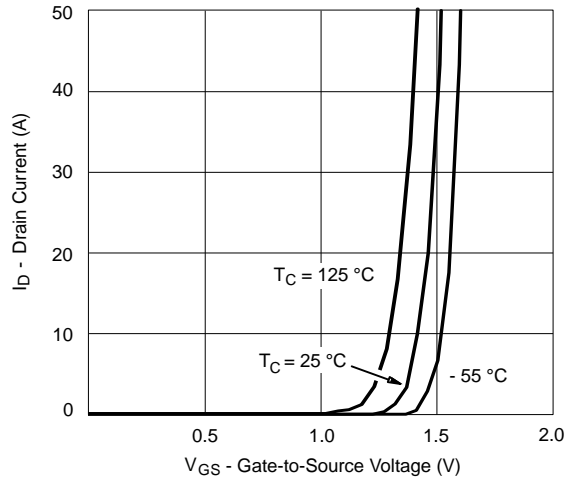
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

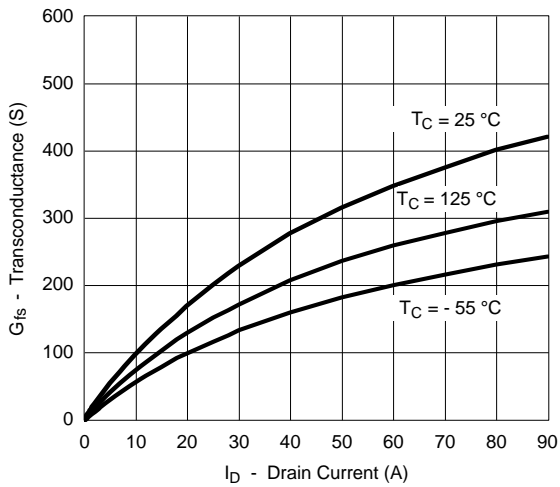
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



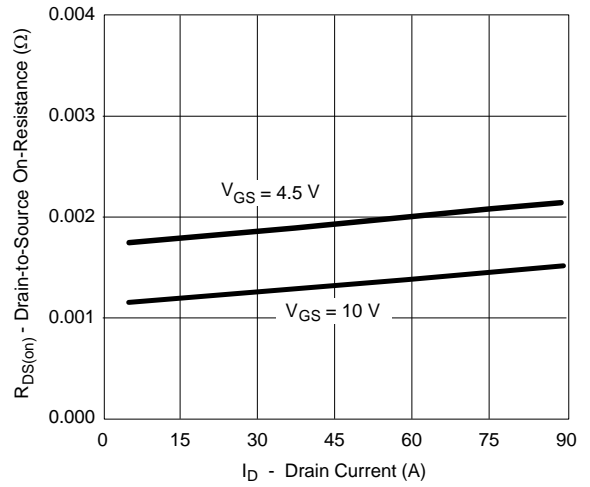
Output Characteristics



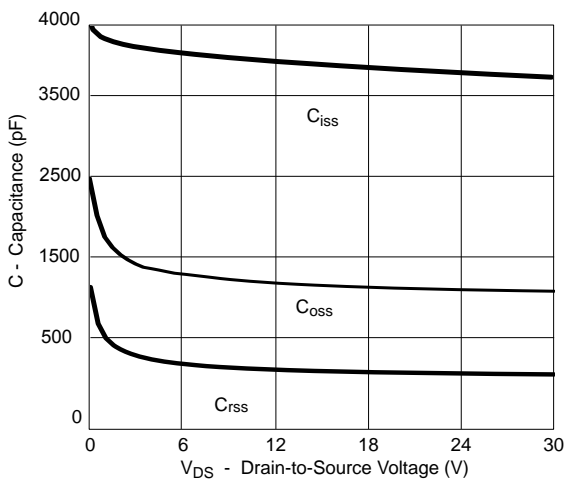
Transfer Characteristics



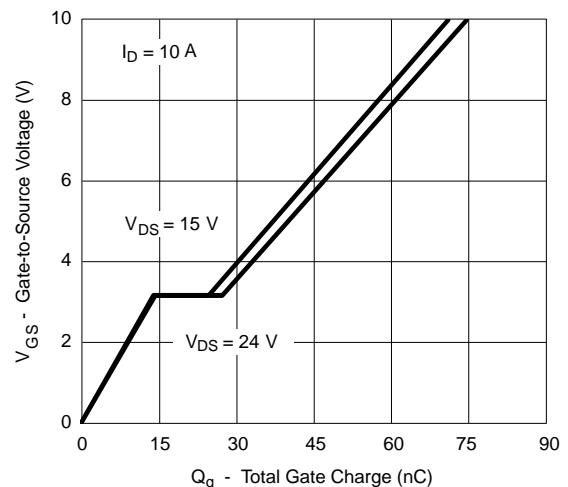
Transconductance



$R_{DS(on)}$ vs. Drain Current

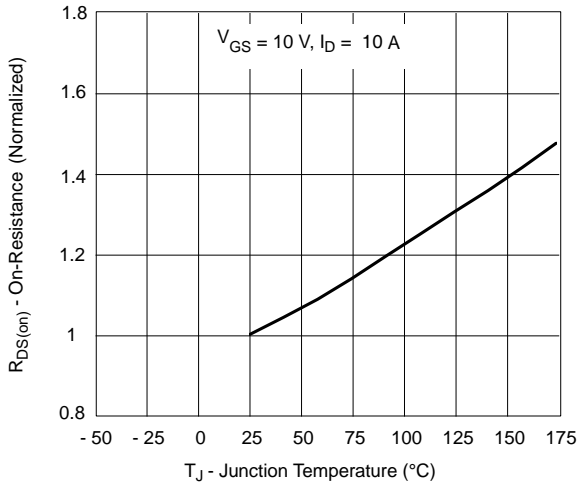


Capacitance

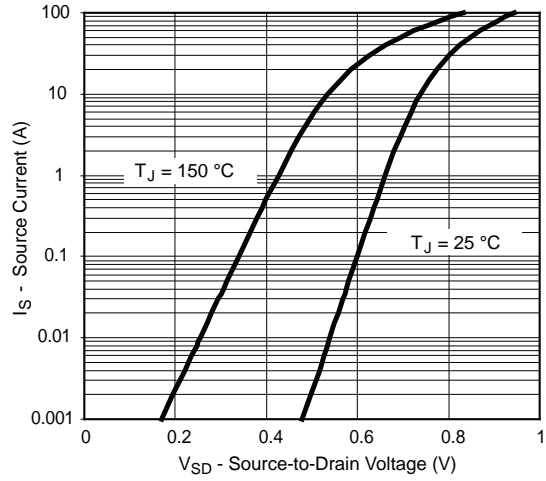


Gate Charge

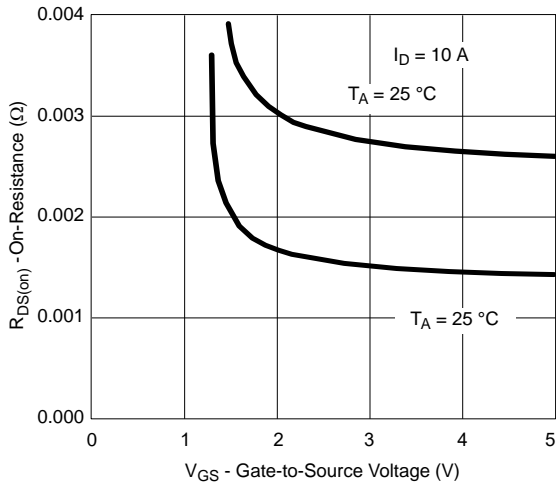
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



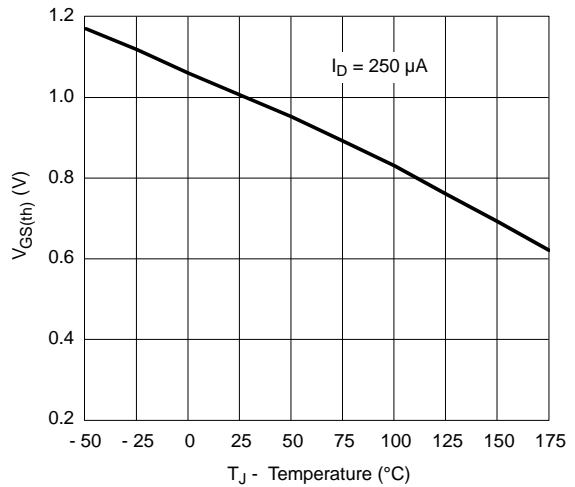
On-Resistance vs. Junction Temperature



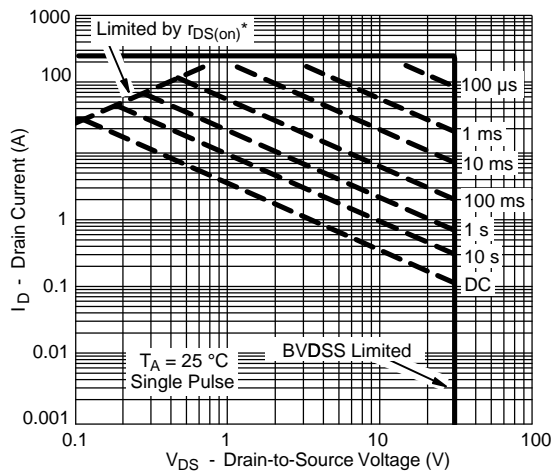
Forward Diode Voltage vs. Temperature



R_{DS(on)} vs. V_{GS} vs. Temperature

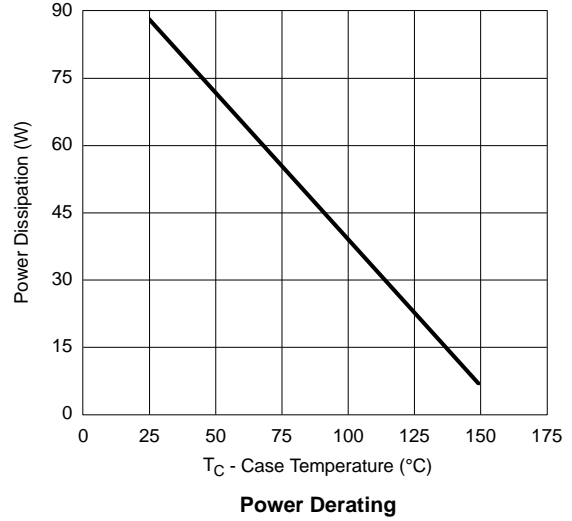
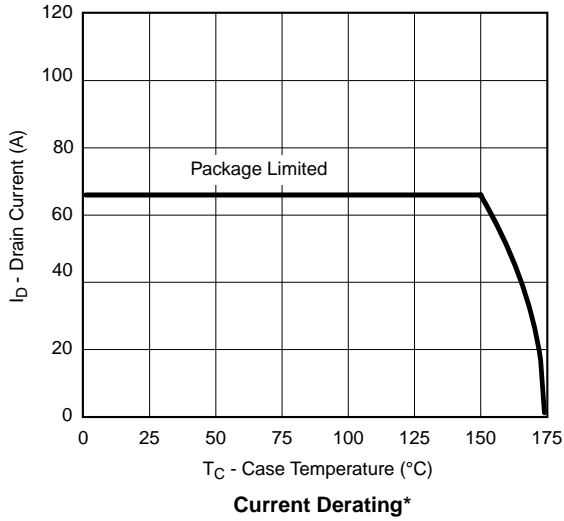


Threshold Voltage

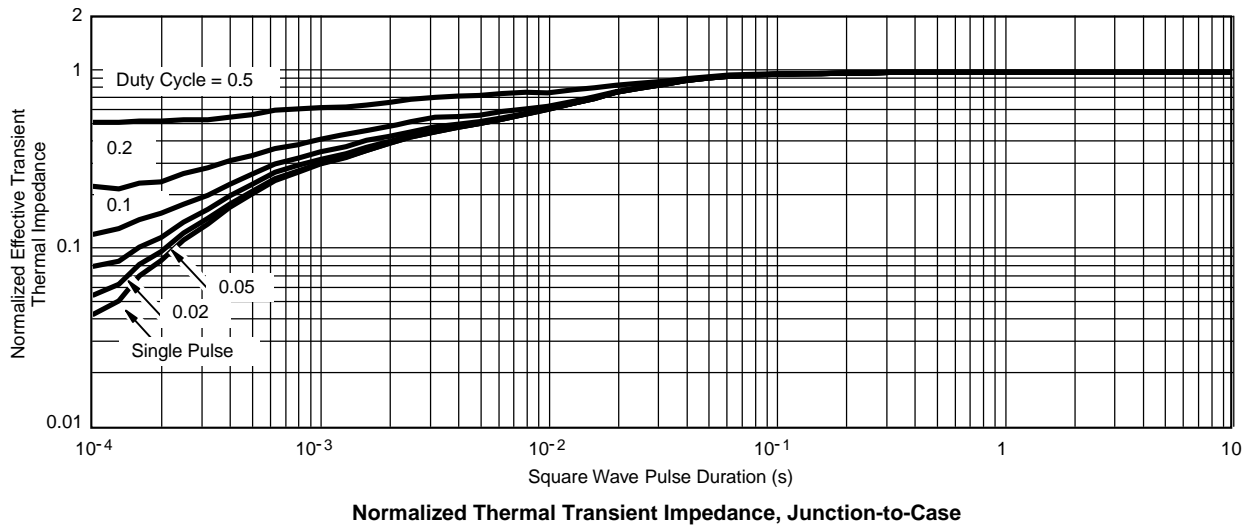


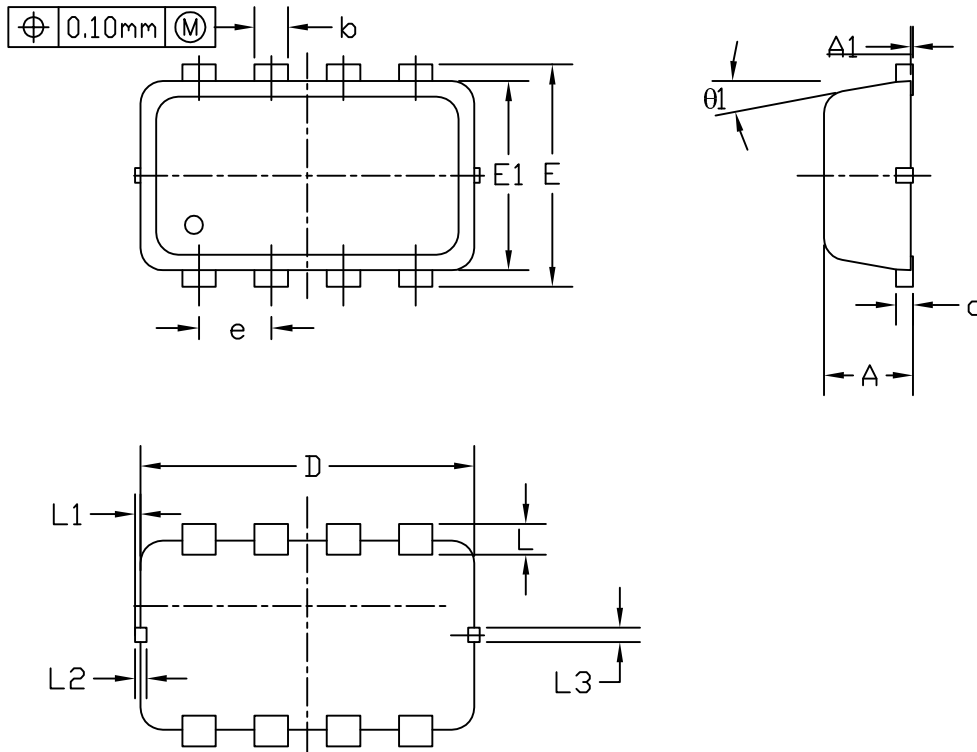
*V_{GS} > minimum V_{GS} at which r_{DS(on)} is specified
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



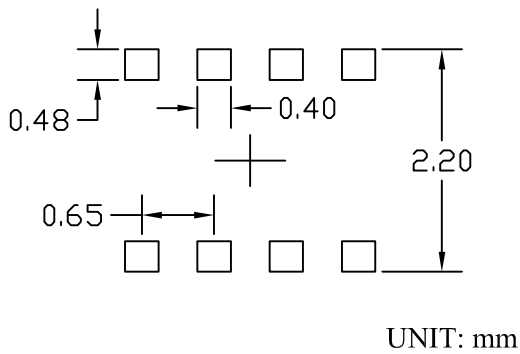
* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





BOTTOM VIEW

RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	—	0.05	0.000	—	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.08	0.15	0.25	0.003	0.006	0.010
D	3.00 BSC			0.118 BSC		
E	2.00 BSC			0.079 BSC		
E1	1.70 BSC			0.067 BSC		
e	0.65 BSC			0.026 BSC		
L	0.20	0.28	0.40	0.008	0.011	0.016
L1	0	—	0.10	0	—	0.004
L2	0.055	0.105	0.155	0.002	0.004	0.006
L3	0.08	0.130	0.180	0.003	0.005	0.007
theta1	0°	10°	12°	0°	10°	12°

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MIL EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
3. TIE BARS ARE CONNECTED TO DRAIN LEADS.

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