

N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A) ^a	Q _g (Typ.)
80	0.0078 at V _{GS} = 10 V	60	24 nC
	0.0160 at V _{GS} = 7.5 V	52	
	0.0310 at V _{GS} = 4.5 V	40	

FEATURES

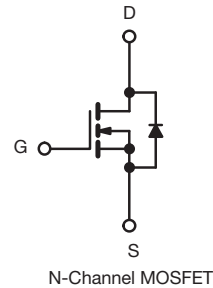
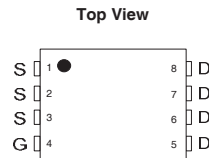
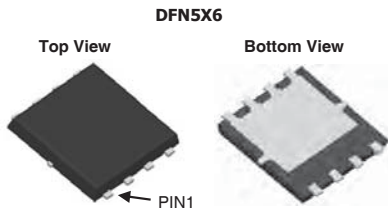
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization:



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Primary Side Switch
- Isolated DC/DC Converters
- Full Bridge
- Synchronous Rectification



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	80	V
Gate-Source Voltage	V _{GS}	± 20	V
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	60 ^a
		T _C = 70 °C	50 ^a
		T _A = 25 °C	20.7 ^{b, c}
		T _A = 70 °C	16.4 ^{b, c}
Pulsed Drain Current (t = 300 μs)	I _{DM}	180	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	60 ^a
		T _A = 25 °C	4.9 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	30	mJ
Single Pulse Avalanche Energy	E _{AS}	45	
Maximum Power Dissipation	P _D	T _C = 25 °C	83
		T _C = 70 °C	53
		T _A = 25 °C	5.4 ^{b, c}
		T _A = 70 °C	3.4 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	18	23	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	1	1.5	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile. The DFN5X6 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 65 °C/W.

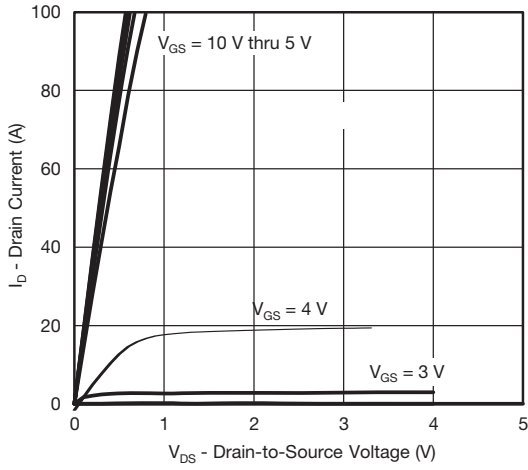
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		37		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		- 5.6			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.5		3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0078	0.0085	Ω
		$V_{GS} = 7.5\text{ V}, I_D = 15\text{ A}$		0.0160	0.0176	
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		0.0310	0.0350	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$		63		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2289		μF
Output Capacitance	C_{oss}		1200			
Reverse Transfer Capacitance	C_{rss}		98			
Total Gate Charge	Q_g	$V_{DS} = 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		47.5	72	nC
		$V_{DS} = 40\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 10\text{ A}$		36.5	55	
Gate-Source Charge	Q_{gs}	$V_{DS} = 40\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		24	36	
Gate-Drain Charge	Q_{gd}		6.8			
Output Charge	Q_{oss}		10.6			
Output Charge	Q_{oss}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		70	105	
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.3	1	2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		13	26	ns
Rise Time	t_r		10	20		
Turn-Off Delay Time	$t_{d(off)}$		41	80		
Fall Time	t_f		9	18		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 7.5\text{ V}, R_g = 1\text{ }\Omega$		16	32	
Rise Time	t_r		16	32		
Turn-Off Delay Time	$t_{d(off)}$		35	70		
Fall Time	t_f		11	22		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			60	A
Pulse Diode Forward Current ^a	I_{SM}				180	
Body Diode Voltage	V_{SD}	$I_S = 5\text{ A}$		0.75	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		46	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}		46	90	nC	
Reverse Recovery Fall Time	t_a		22		ns	
Reverse Recovery Rise Time	t_b		24			

Notes:

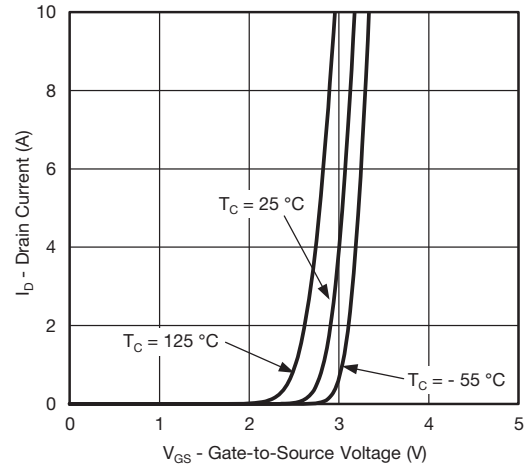
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

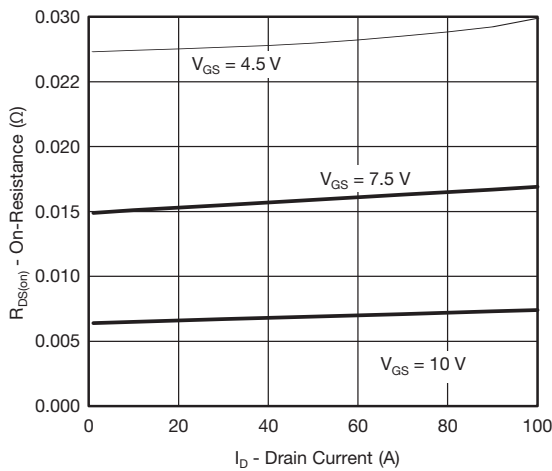
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



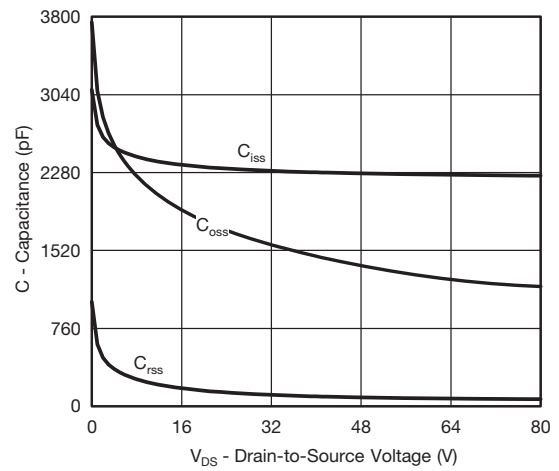
Output Characteristics



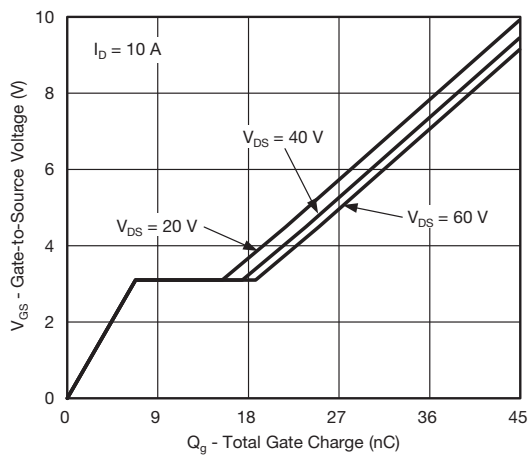
Transfer Characteristics



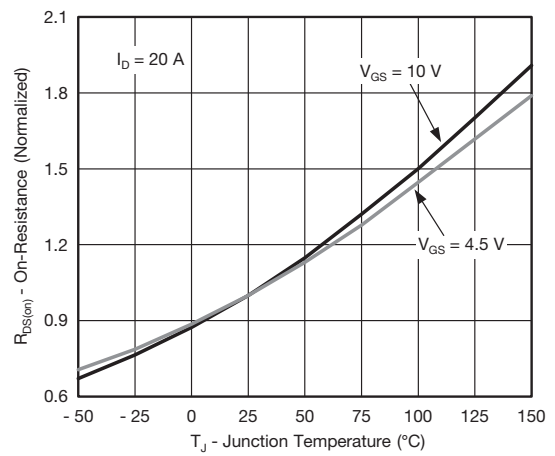
On-Resistance vs. Drain Current



Capacitance

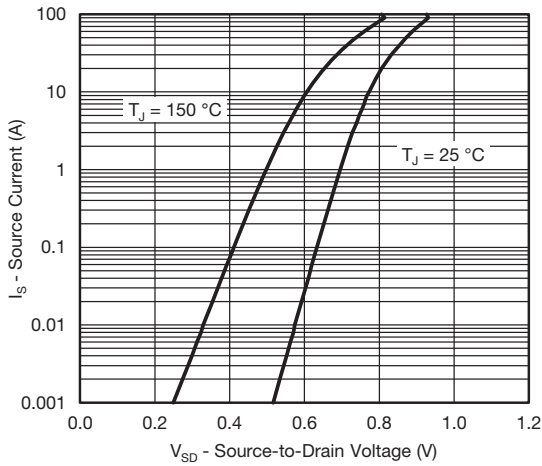


Gate Charge

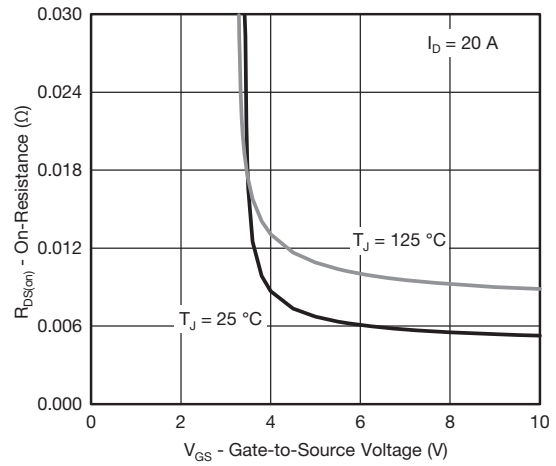


On-Resistance vs. Junction Temperature

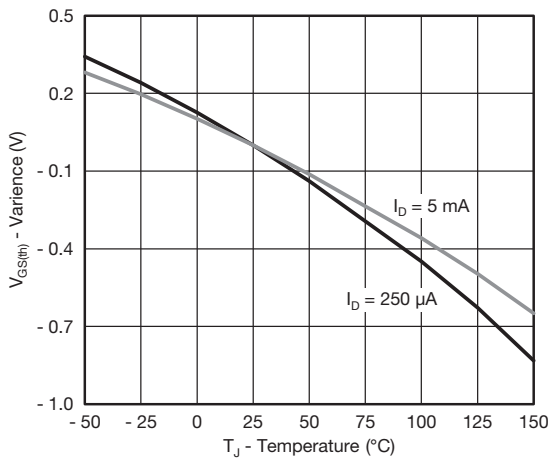
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



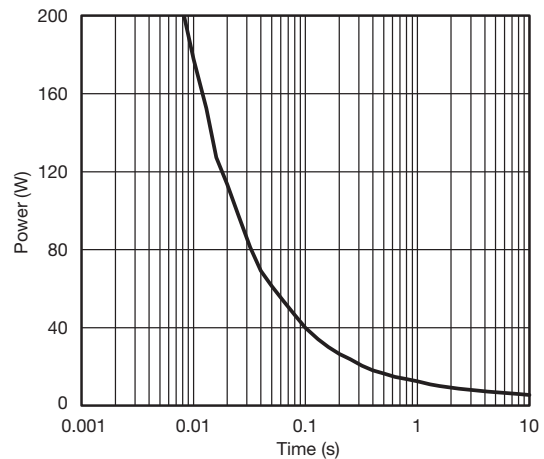
Source-Drain Diode Forward Voltage



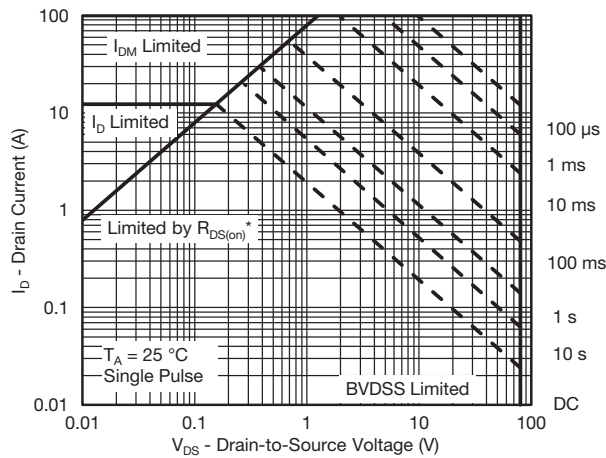
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

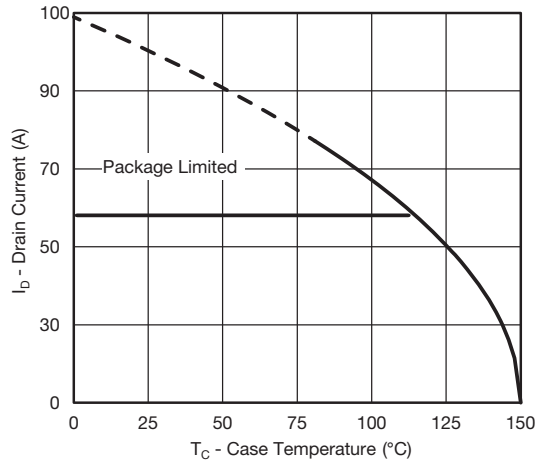


Single Pulse Power, Junction-to-Ambient

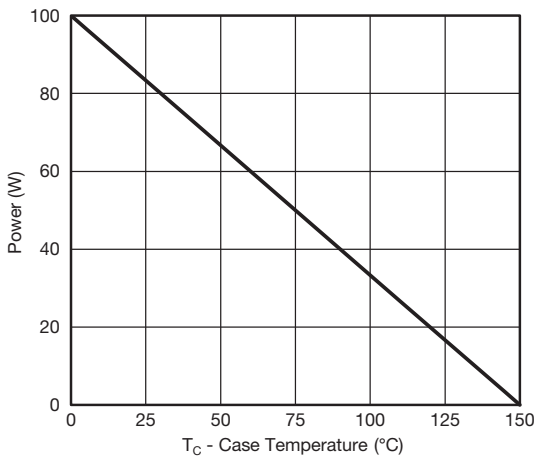


Safe Operating Area, Junction-to-Ambient

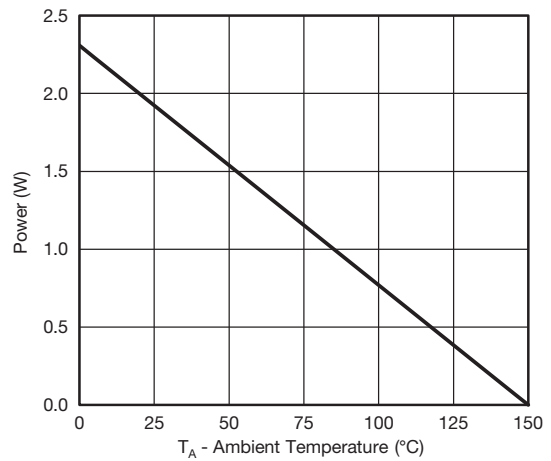
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



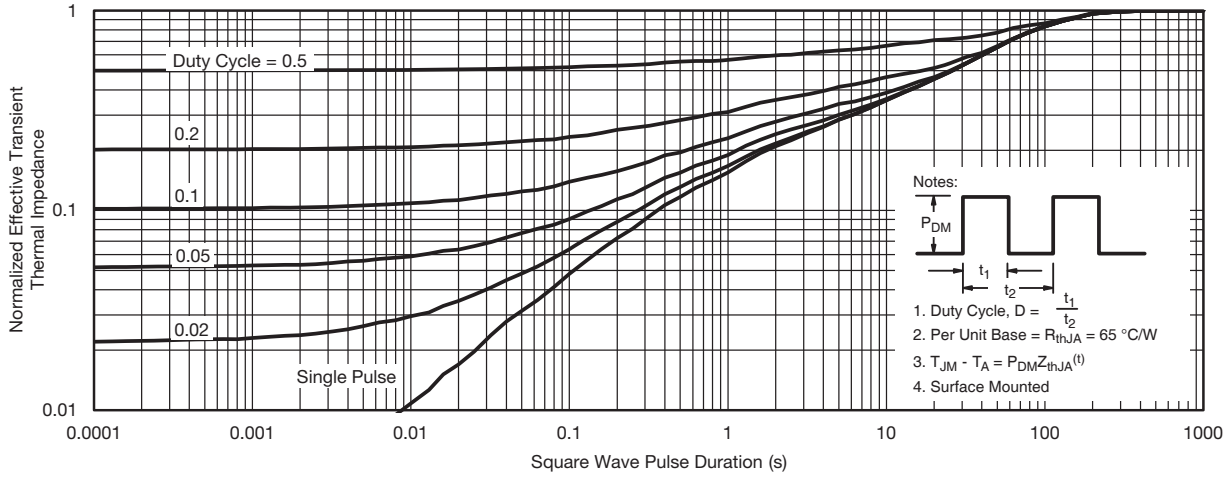
Power, Junction-to-Case



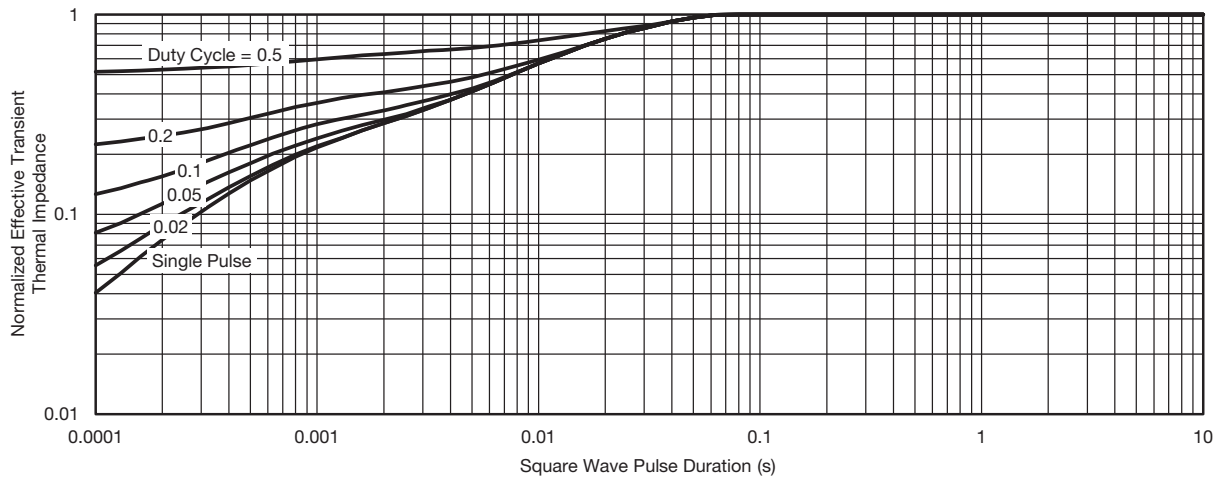
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

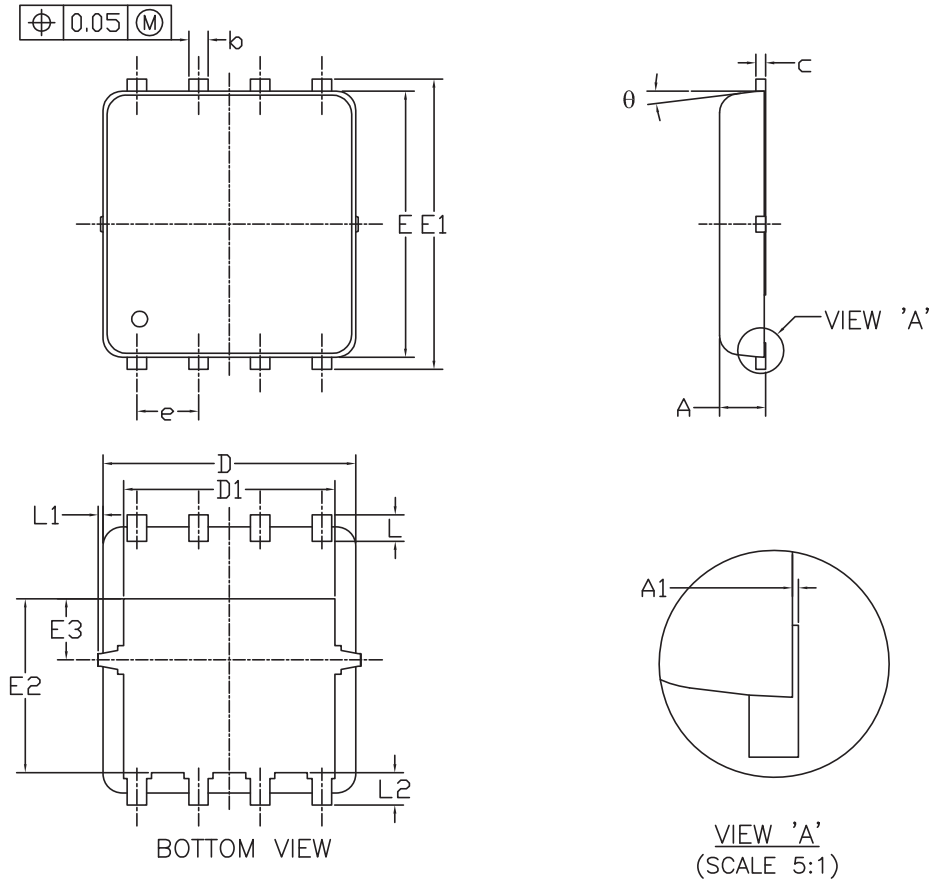


Normalized Thermal Transient Impedance, Junction-to-Ambient



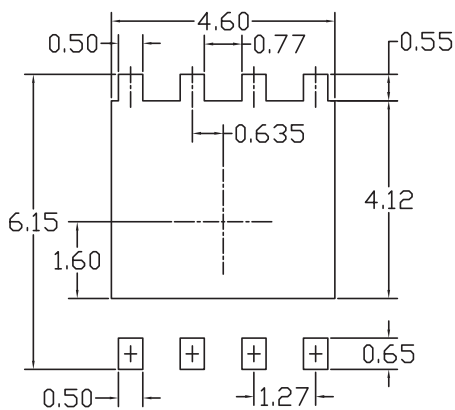
Normalized Thermal Transient Impedance, Junction-to-Case

DFN5x6_8L_EP1_P PACKAGE OUTLIN



VIEW 'A'
(SCALE 5:1)

RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
θ	0°	---	10°	0°	---	10°

UNIT: mm

NOTE

- PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
- CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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