Process Introduction

2um / 18V Bipolar Process Technology

Process features

- Up-down isolation
- 8um space from Base to Iso
- Deep N+ collector plug
- NPN transistor
- Lateral PNP transistor
- Implant resistor (optional)
- MOS capacitor
- Double metal (optional)
- Applications: analog, power linear

Key Design Rules

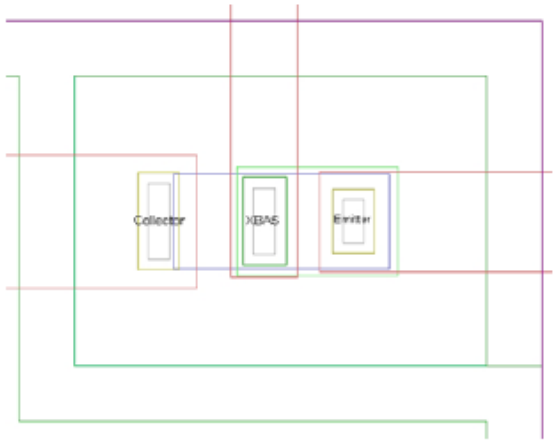
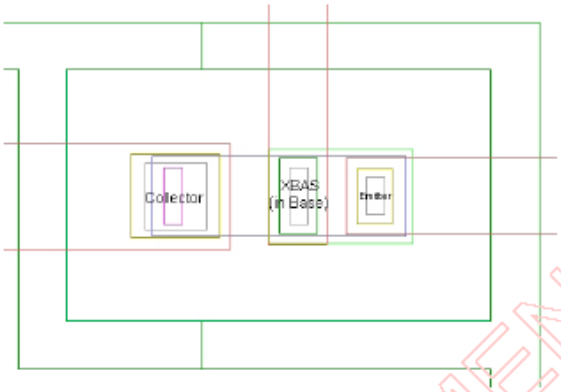
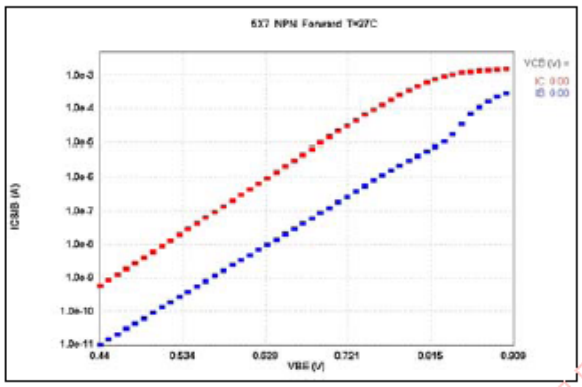
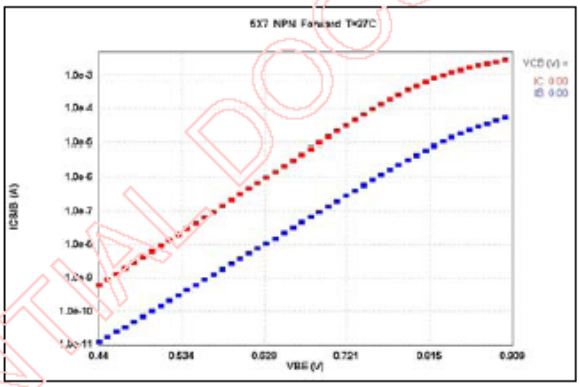
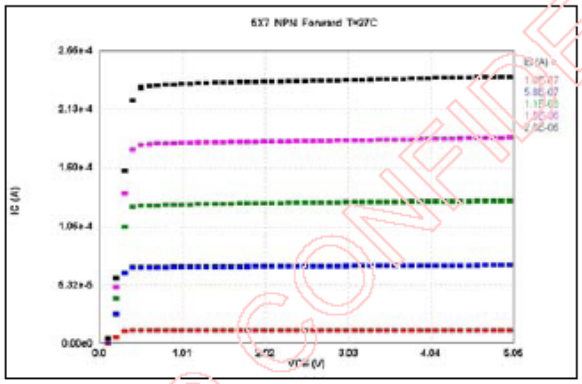
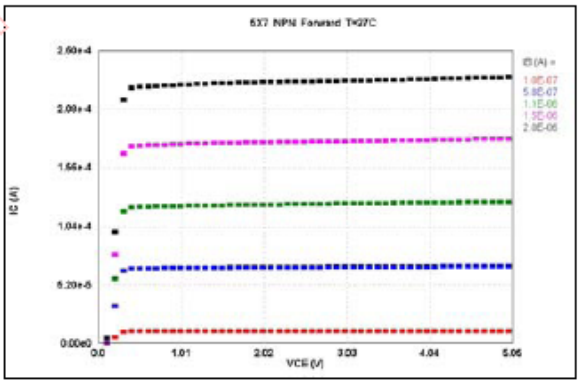
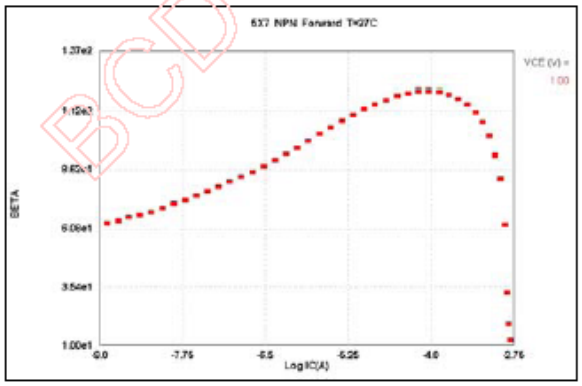
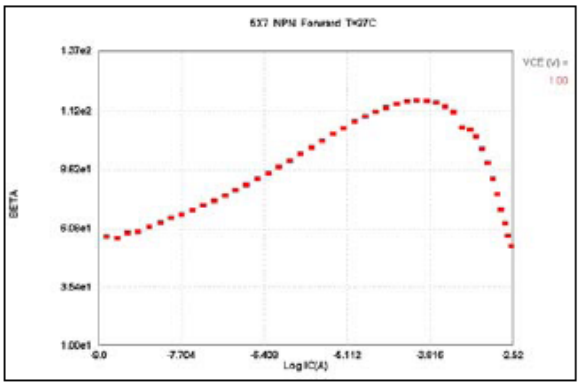
10 Masks	Min. Width/Space(um)
Diffusion	4
Contact	2
Metal	3/2

Electrical Specification

Device	Parameter	Specification			
		Min	Typ	Max	Unit
NPN（5x7um^{2}emitter）	Hfe(Ic=100uA)	80	140	250	-
	BVceo(Ic=10uA)	18	35	-	V
	BVebo(I=10uA)	6.8	7.3	7.8	V
PBASE-LPNP (Wb=8um)	Hfe(Ic=10uA)	100	250	400	-
	BVceo(Ic=10uA)	18	40	-	V
XBASE-LPNP (Wb=10um)	Hfe(Ic=10uA)	200	500	800	-
	BVceo(Ic=10uA)	18	40	-	V
Sheet Resistance(20x200um^2)	PBASE-R	190	215	240	Ω/□
	Implant-R	1.84	2.3	2.76	kΩ/□
Capacitance (Si_3N_4)	C(100x100um^2)	8.5	10.6	12.7	pF

Process Introduction

Device characteristic curve

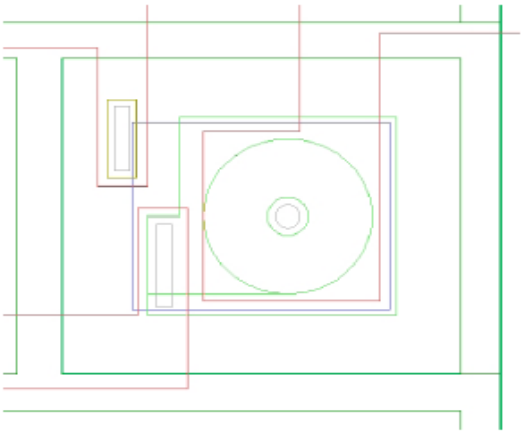
NPN 5×7 without DN	NPN 5×7 with DN
Layout	**Layout**
	
I-V curve	**I-V curve**
	
	
	

Process Introduction

PBAS LPNP

ϕ=7.0 um, W_b=8.0 um

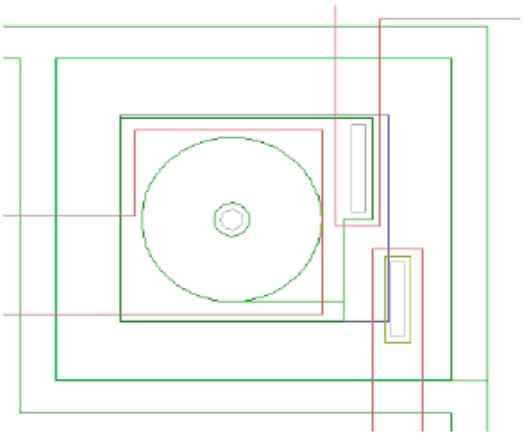
Layout



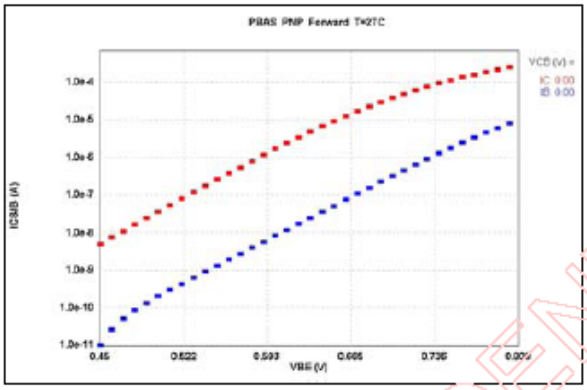
XBAS LPNP

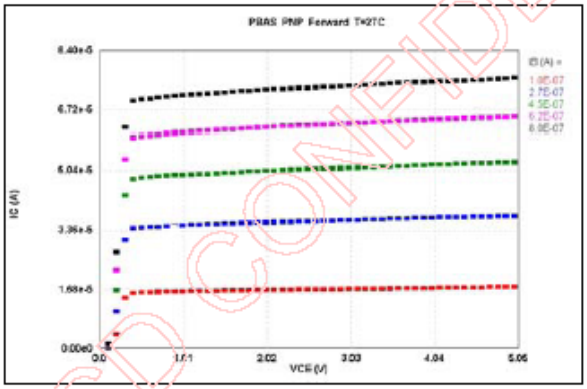
ϕ=5.0 um, W_b=10.0 um

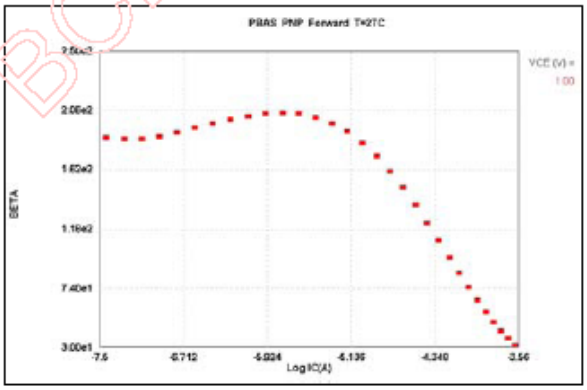
Layout



I-V curve







I-V curve