DTK75N80-A

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N-Channel 85 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (mΩ) Typ.	I_D (A)	Q_g (Typ.)
85	4.9 at V_{GS} = 10 V	110[a]	65 nC

FEATURES

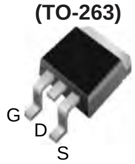
- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested

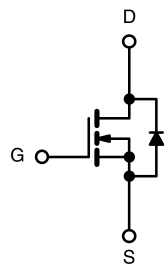
RoHS COMPLIANT

APPLICATIONS

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting

D²PAK (TO-263)





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	85	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	110[a]	A
	T_C = 70 °C		102	
	T_A = 25 °C		39[b, c]	
	T_A = 70 °C		33[b, c]	
Pulsed Drain Current (t = 100 µs)		I_{DM}	440	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	110[a]	
	T_A = 25 °C		39[b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	107	
Single Pulse Avalanche Energy		E_{AS}	690	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	355	W
	T_C = 70 °C		167	
	T_A = 25 °C		10[b, c]	
	T_A = 70 °C		7[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, f]	t ≤ 10 s	R_{thJA}	12	15	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	0.3	0.5	

Notes

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. The TO-263 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 70 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	85			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA		38		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2		4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =85 V, V_{GS} = 0 V			1	μA
		V_{DS} = 85 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	110			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		4.9	6.9	mΩ
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 20 A		63		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		6055		pF
Output Capacitance	C_{oss}			2250		
Reverse Transfer Capacitance	C_{rss}			68		
Total Gate Charge	Q_g	V_{DS} = 40 V,V_{GS} = 10 V, I_D = 20 A		65	120	nC
Gate-Source Charge	Q_{gs}			23		
Gate-Drain Charge	Q_{gd}			7		
Output Charge	Q_{oss}	V_{DS} = 40 V, V_{GS} = 0 V		186		
Gate Resistance	R_g	f = 1 MHz	1	2	5	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 4 Ω $I_D \cong$ 20 A, V_{GEN} = 10 V, R_g = 1 Ω		25		ns
Rise Time	t_r			12		
Turn-Off DelayTime	$t_{d(off)}$			53		
Fall Time	t_f			18		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 4 Ω $I_D \cong$ 20 A, V_{GEN} = 6.0 V, R_g = 1 Ω		15		
Rise Time	t_r			13		
Turn-Off DelayTime	$t_{d(off)}$			34		
Fall Time	t_f			8		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			110	A
Pulse Diode Forward Current (t = 100 μs)	I_{SM}				440	
Body Diode Voltage	V_{SD}	I_S = 1 A		0.68	1	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20 A, dI/dt = 500 A/μs, T_J = 25 °C		36		ns
Body Diode Reverse Recovery Charge	Q_{rr}			57		nC
Reverse Recovery Fall Time	t_a			28		ns
Reverse Recovery Rise Time	t_b			20		

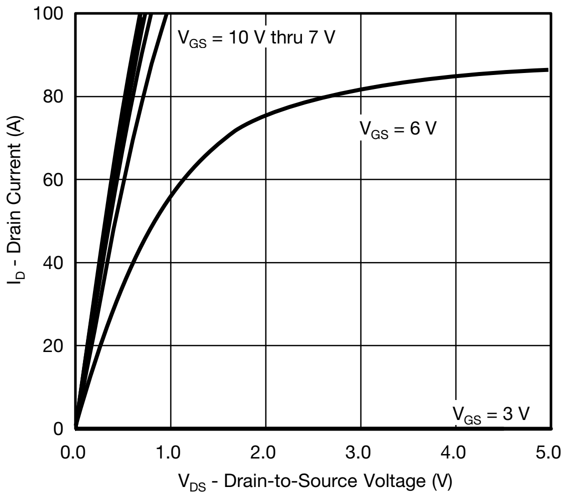
Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

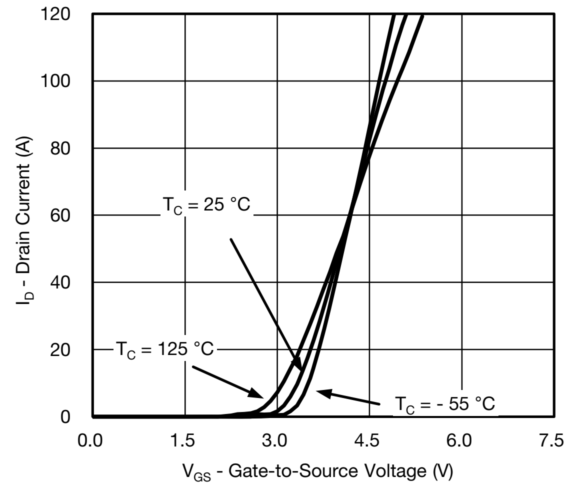
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

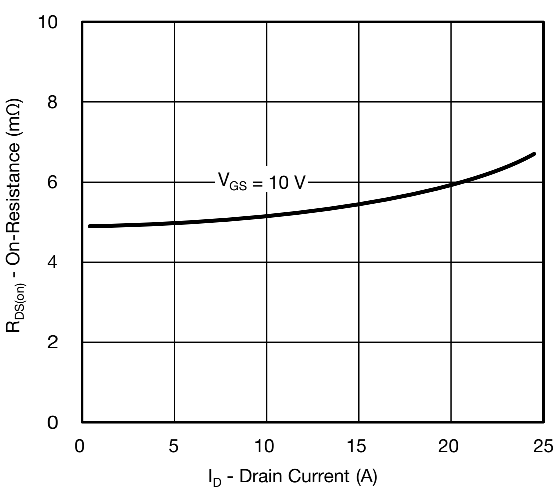
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



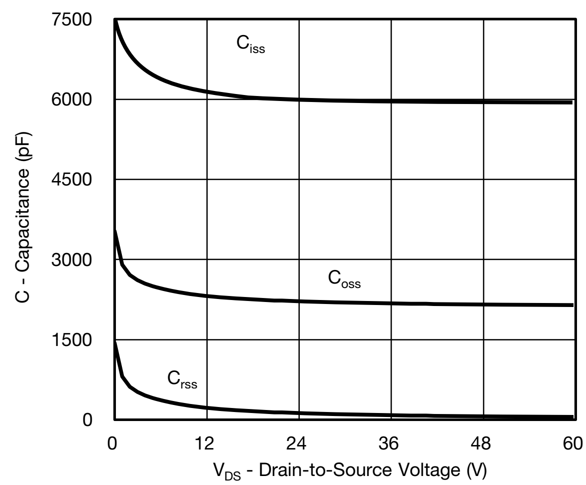
Output Characteristics



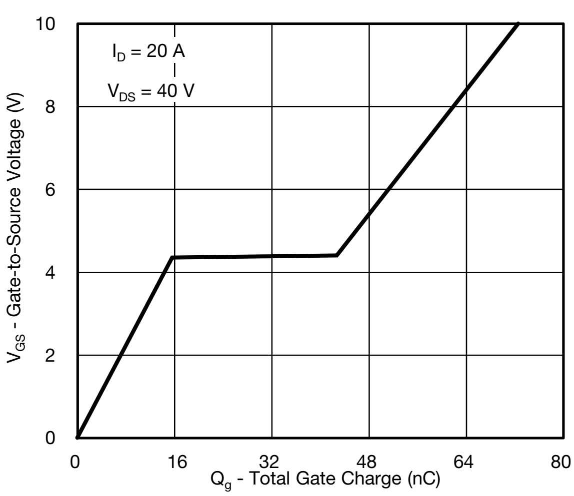
Transfer Characteristics



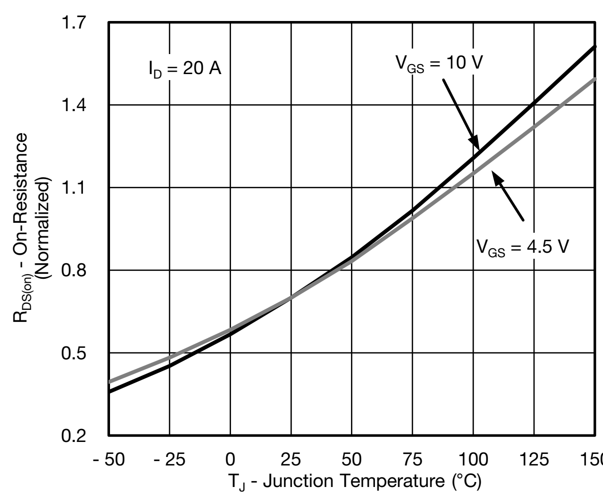
On-Resistance vs. Drain Current



Capacitance

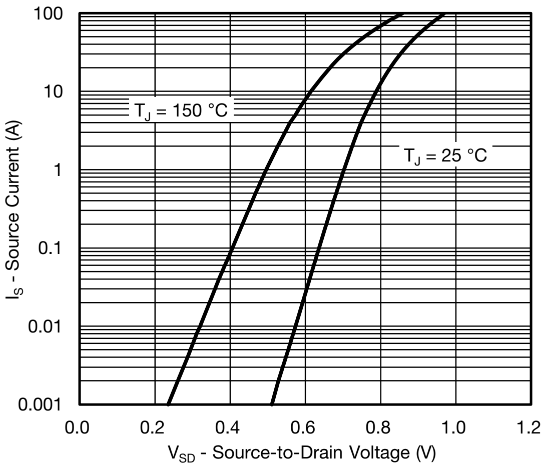


Gate Charge

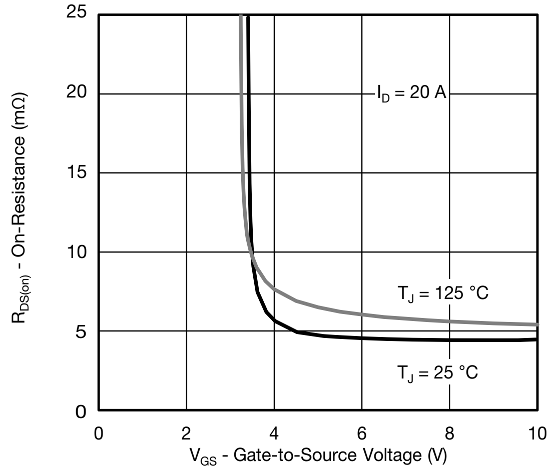


On-Resistance vs. Junction Temperature

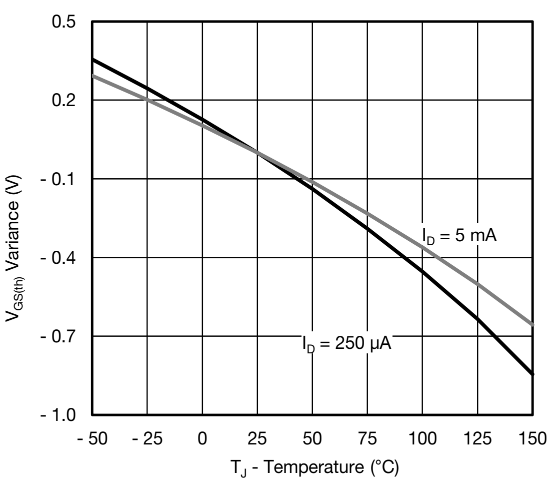
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



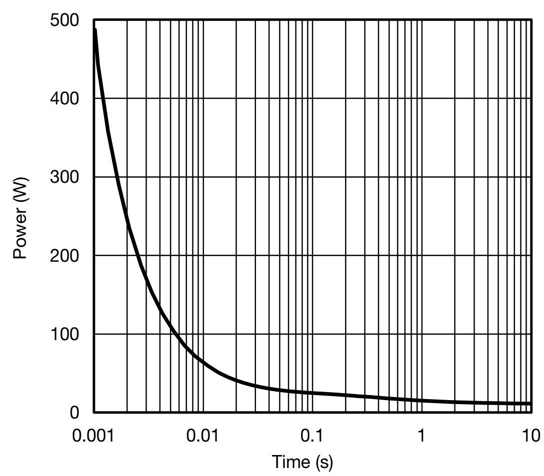
Source-Drain Diode Forward Voltage



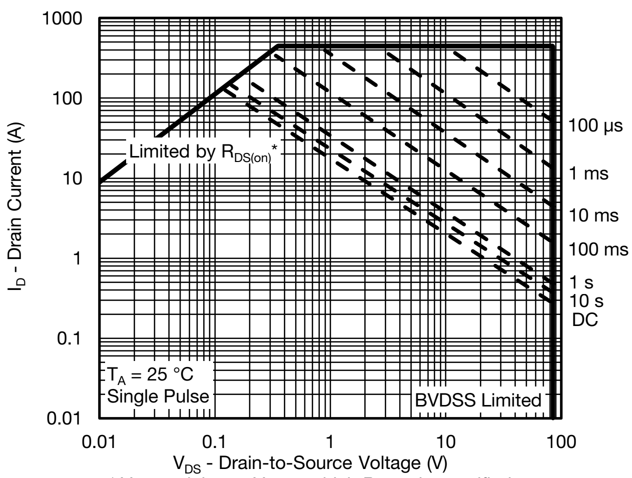
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



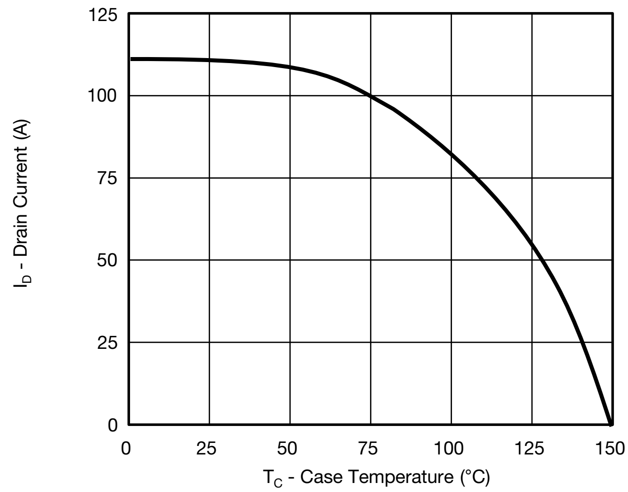
Single Pulse Power, Junction-to-Ambient



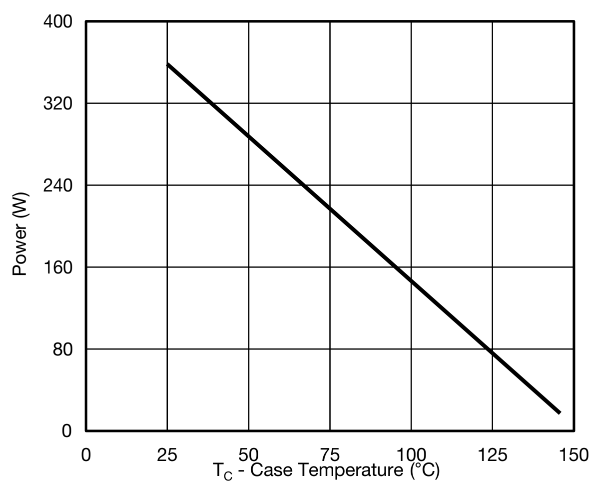
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

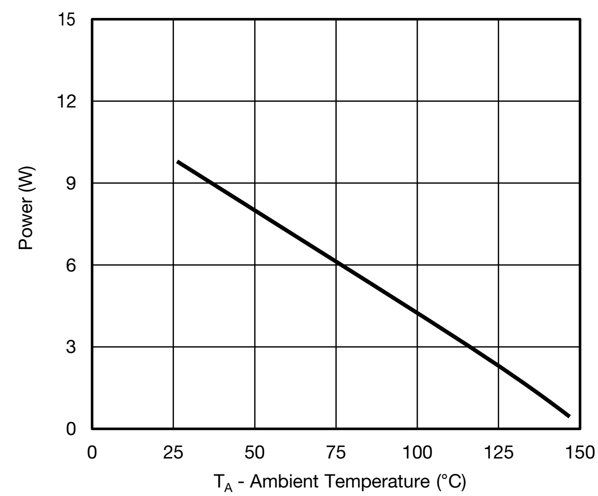
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



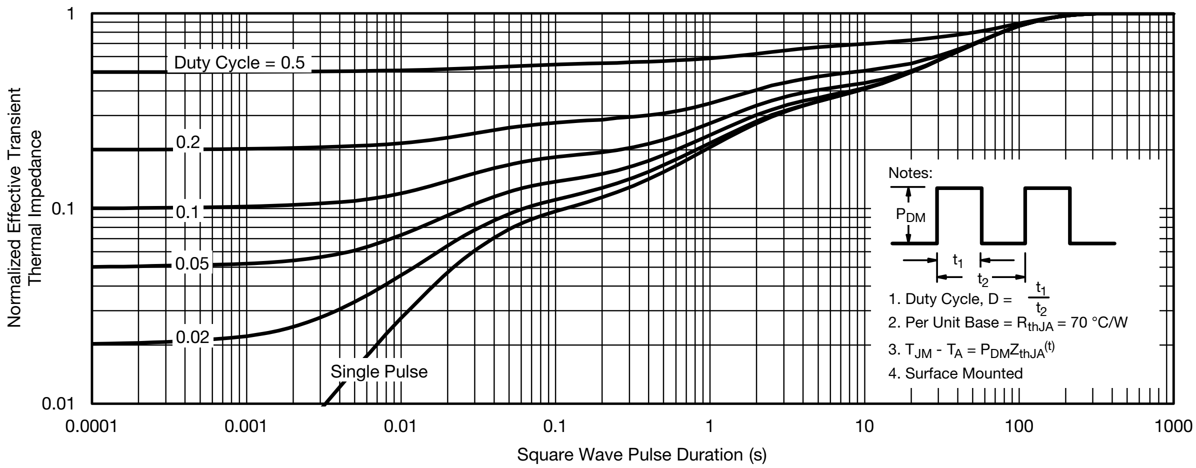
Power, Junction-to-Case



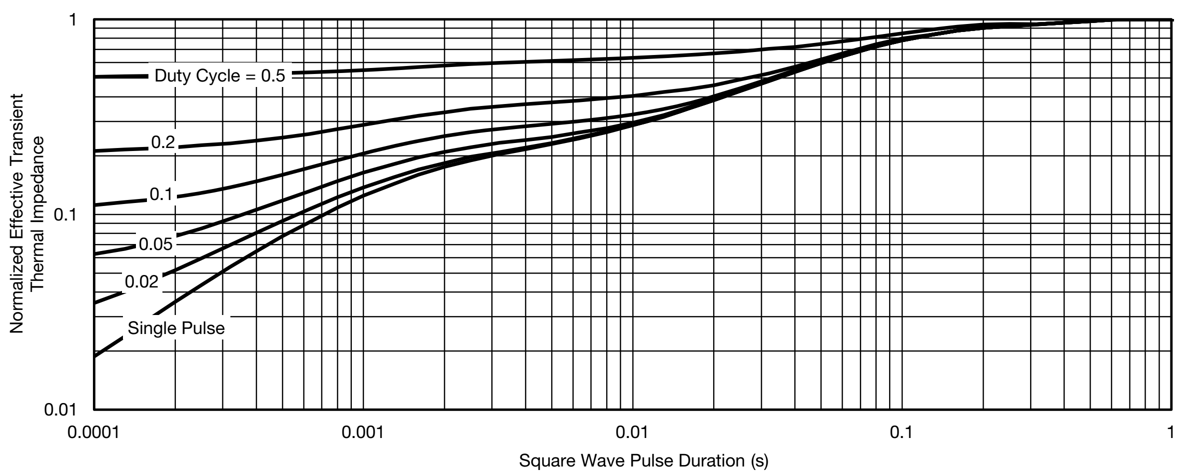
Power, Junction-to-Ambient

** The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.*

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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