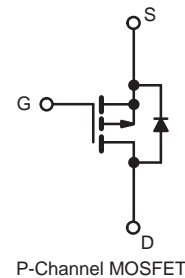
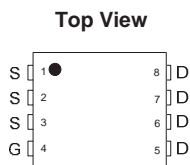
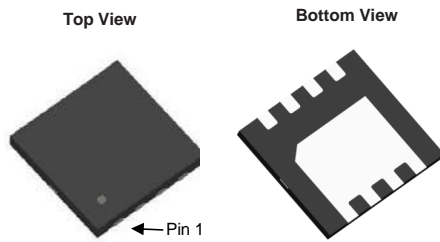


P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
- 30	0.0123 at V _{GS} = - 10 V	- 45 ^d	40 nC
	0.0179 at V _{GS} = - 4.5 V	- 30 ^d	

DFN 3x3 EP



FEATURES

- DT-Trench Power MOSFET
- Low On-Resistance for Low Voltage Drop
- 100 % R_g and UIS Tested

APPLICATIONS

- Battery, Load and Adaptor Switches
 - Notebook Computers
 - Notebook Battery Packs


RoHS
 COMPLIANT

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	- 45 ^d	A
	T _C = 70 °C	- 35 ^d	
	T _A = 25 °C	- 18 ^{a, b}	
	T _A = 70 °C	- 9 ^{a, b}	
Pulsed Drain Current (t = 100 μs)	I _{DM}	- 180	
Continuous Source-Drain Diode Current	T _C = 25 °C	- 45 ^d	
	T _A = 25 °C	- 3.8 ^{a, b}	
Avalanche Current	L = 0.1 mH	- 25	
Single-Pulse Avalanche Energy	E _{AS}	35	mJ
Maximum Power Dissipation	T _C = 25 °C	43	W
	T _C = 70 °C	26	
	T _A = 25 °C	4.8 ^{a, b}	
	T _A = 70 °C	3 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R _{thJA}	25	30	°C/W
Maximum Junction-to-Case	R _{thJC}	2.5	3	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. Maximum under steady state conditions is 70 °C/W.

d. Package limited.

e. The DFN3X3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

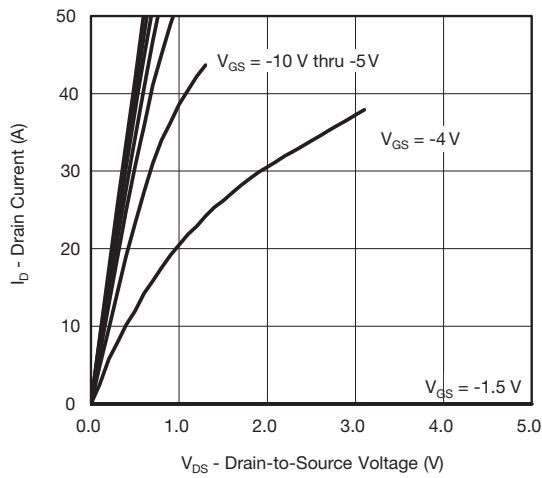
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = - 250 μA	- 30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 22		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			4.1		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1		- 3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 24 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 24 V, V _{GS} = 0 V, T _J = 55 °C			- 5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 10 V, V _{GS} = - 10 V	- 180			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 15 A		0.0123	0.014	Ω
		V _{GS} = - 4.5 V, I _D = - 10 A		0.0179	0.02	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 15 A		60		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 24 V, V _{GS} = 0 V, f = 1 MHz		3150		pF
Output Capacitance	C _{oss}			975		
Reverse Transfer Capacitance	C _{rss}			384		
Total Gate Charge	Q _g	V _{DS} = - 24 V, V _{GS} = - 10 V, I _D = - 10 A		92		nC
Gate-Source Charge	Q _{gs}	V _{DS} = - 24 V, V _{GS} = - 4.5 V, I _D = - 10 A		41		
Gate-Drain Charge	Q _{gd}			14		
				29		
Gate Resistance	R _g	f = 1 MHz	0.5	2.9	5.8	Ω
Turn-On Delay Time	t _{d(on)}	V _{DS} = - 15 V, R _L = 1.5 Ω I _D ≅ - 10 A, V _{GS} = - 10 V, R _g = 1 Ω		16		ns
Rise Time	t _r			14		
Turn-Off DelayTime	t _{d(off)}			60		
Fall Time	t _f			12		
Turn-On Delay Time	t _{d(on)}	V _{DS} = - 15 V, R _L = 1.5 Ω I _D ≅ - 10 A, V _{GS} = - 4.5 V, R _g = 1 Ω		60		
Rise Time	t _r			59		
Turn-Off DelayTime	t _{d(off)}			50		
Fall Time	t _f			22		
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 45	A
Pulse Diode Forward Current (100 μs)	I _{SM}				- 180	
Body Diode Voltage	V _{SD}	I _S = - 3 A, V _{GS} = 0		- 0.7	- 1.20	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 10 A, dI/dt = 100 A/μs, T _J = 25 °C		22		ns
Body Diode Reverse Recovery Charge	Q _{rr}			12		nC
Reverse Recovery Fall Time	t _a			9		ns
Reverse Recovery Rise Time	t _b			13		

Notes:

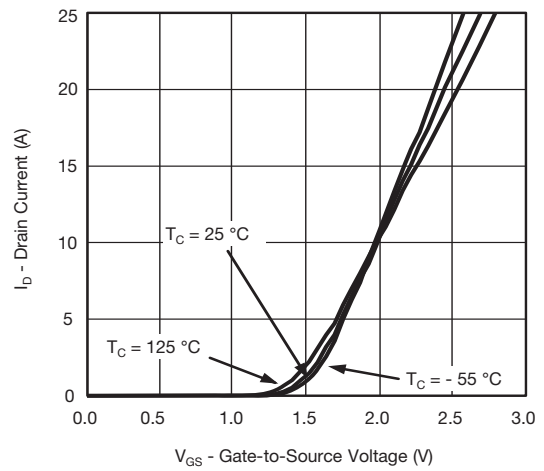
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

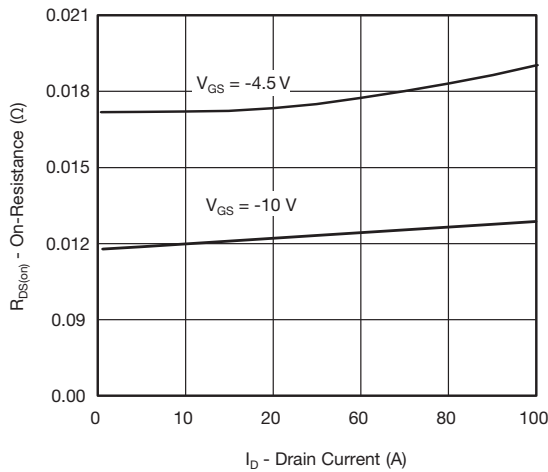
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



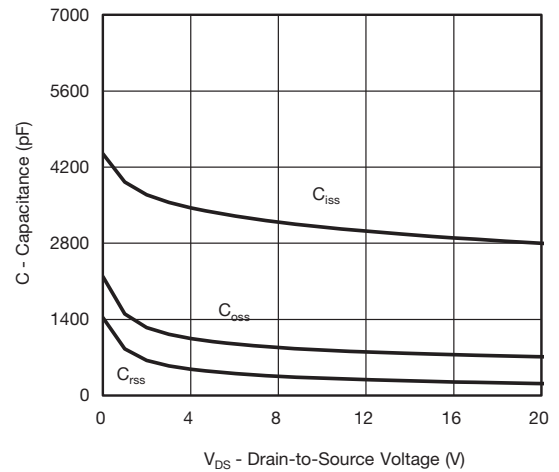
Output Characteristics



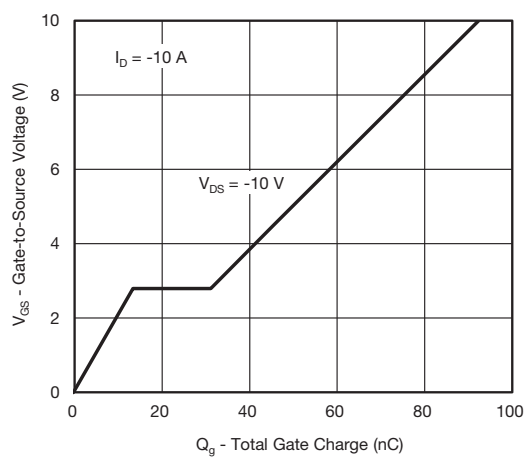
Transfer Characteristics



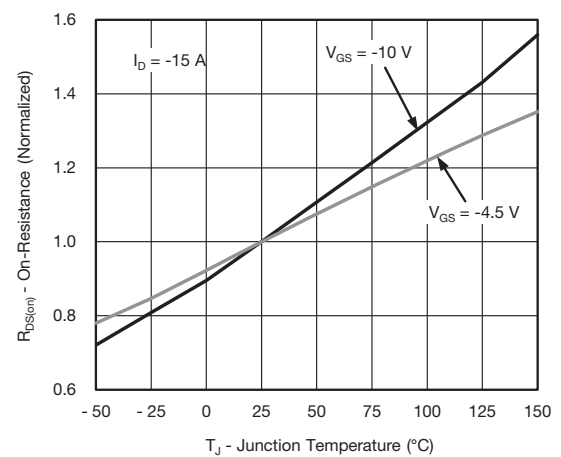
On-Resistance vs. Drain Current



Capacitance

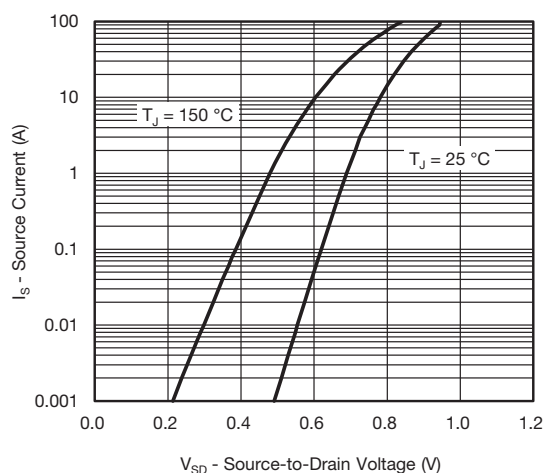


Gate Charge

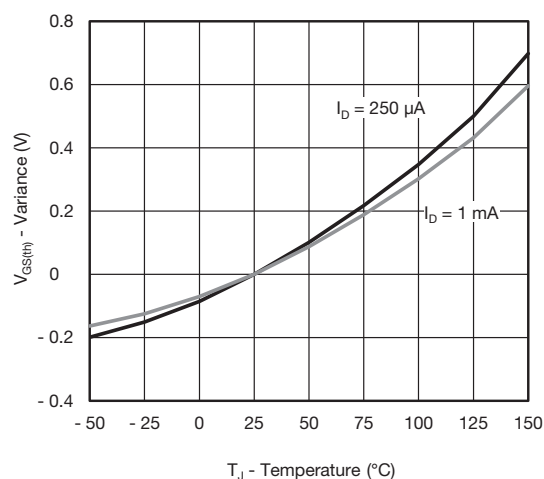


On-Resistance vs. Junction Temperature

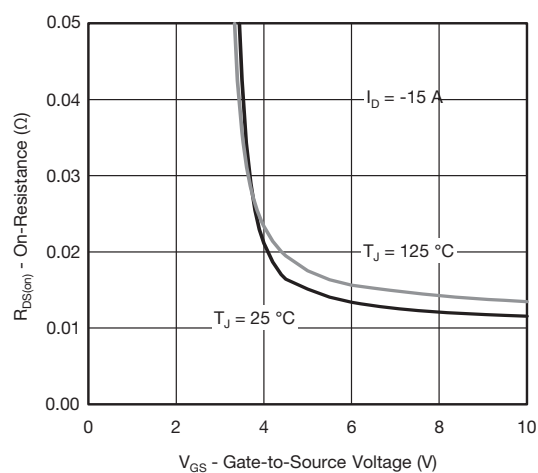
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



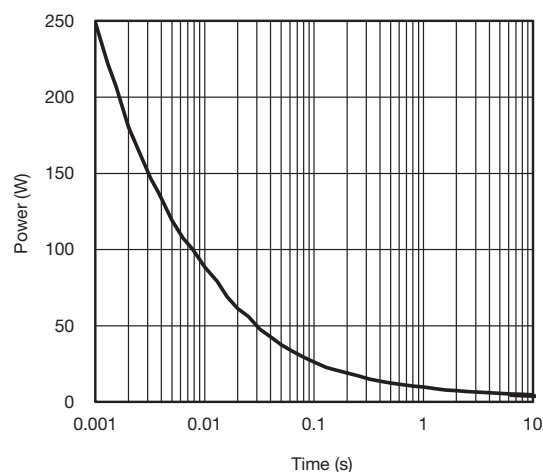
Source-Drain Diode Forward Voltage



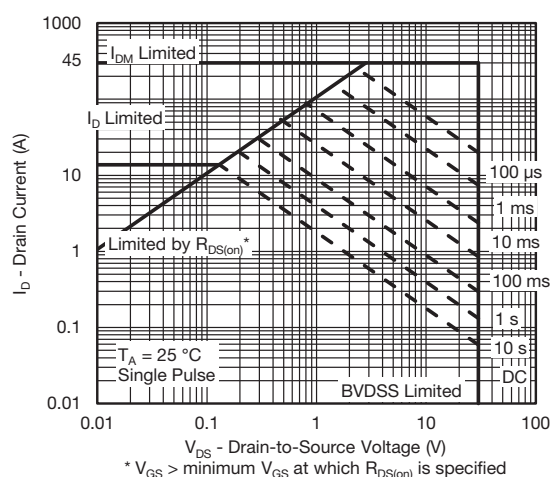
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

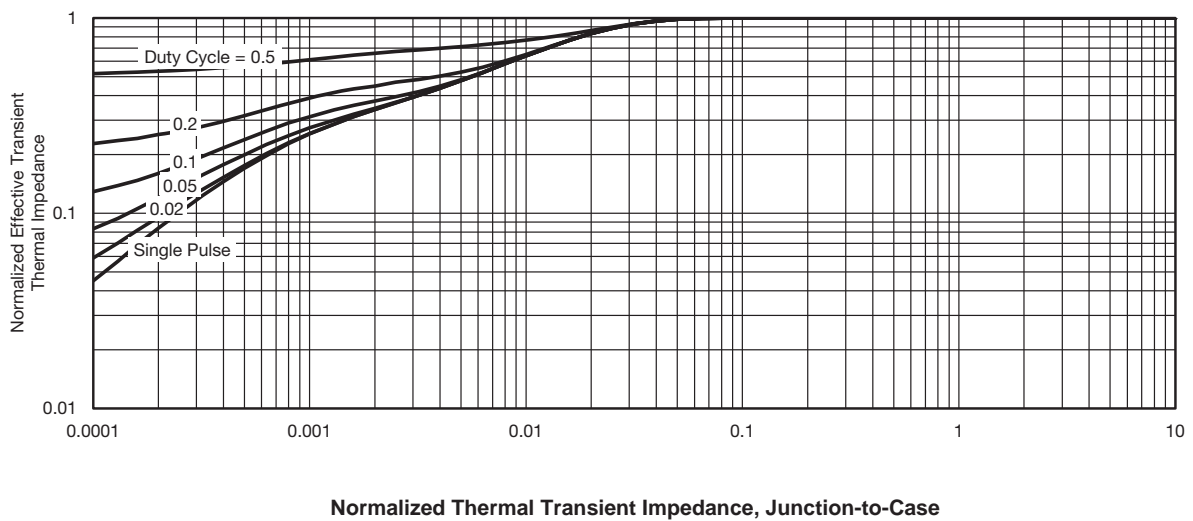
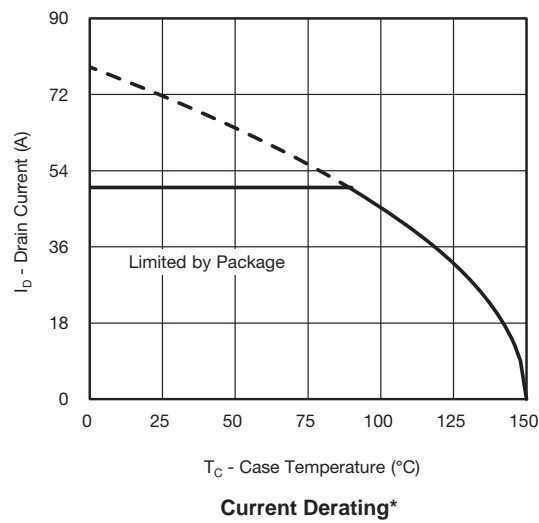


Single Pulse Power, Junction-to-Ambient



Safe Operating Area

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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