

P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)(Typ.)	I_D (A)	Q_g (Typ.)
- 30	12.3at $V_{GS} = - 10$ V	- 45 ^d	41 nC
	17.9at $V_{GS} = - 4.5$ V	- 30 ^d	

FEATURES

- DT-Trench Power MOSFET
- Low On-Resistance for Low Voltage Drop
- 100 % R_g and UIS Tested

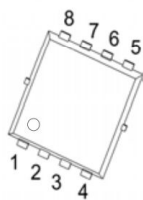
APPLICATIONS

- Battery, Load and Adaptor Switches
 - Notebook Computers
 - Notebook Battery Packs

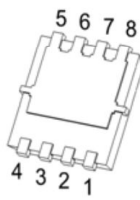

RoHS
 COMPLIANT

PDFN 3.3x3.3

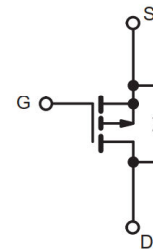
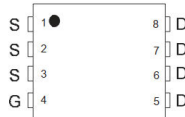
Top View



Bottom View



Top View



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	- 45 ^d	A
	$T_C = 70$ °C	- 35 ^d	
	$T_A = 25$ °C	- 18 ^{a, b}	
	$T_A = 70$ °C	- 9 ^{a, b}	
Pulsed Drain Current ($t = 100$ μ s)	I_{DM}	- 180	A
Continuous Source-Drain Diode Current	$T_C = 25$ °C	- 45 ^d	
	$T_A = 25$ °C	- 3.8 ^{a, b}	
Avalanche Current	I_{AS}	- 25	mJ
Single-Pulse Avalanche Energy	E_{AS}	35	
Maximum Power Dissipation	$T_C = 25$ °C	43	W
	$T_C = 70$ °C	26	
	$T_A = 25$ °C	4.8 ^{a, b}	
	$T_A = 70$ °C	3 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R_{thJA}	25	30	°C/W
Maximum Junction-to-Case	R_{thJC}	2.5	3	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

 b. $t = 10$ s.

c. Maximum under steady state conditions is 70 °C/W.

d. Package limited.

e. The PDFN3.3X3.3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = - 250 μA	- 30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 22		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			4.1		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1		- 3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 30 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 24 V, V _{GS} = 0 V, T _J = 55 °C			- 5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 10 V, V _{GS} = - 10 V	- 45			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 15 A		12.3	14	mΩ
		V _{GS} = - 4.5 V, I _D = - 10 A		17.9	20	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 15 A		60		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		2260		pF
Output Capacitance	C _{oss}			260		
Reverse Transfer Capacitance	C _{rss}			254		
Total Gate Charge	Q _g	V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 15 A		41		nC
Gate-Source Charge	Q _{gs}			14		
Gate-Drain Charge	Q _{gd}			29		
Gate Resistance	R _g	f = 1 MHz		11		Ω
Turn-On Delay Time	t _{d(on)}	V _{DS} = - 15 V, R _L = 1.5 Ω I _D ≅ - 15 A, V _{GS} = - 10 V, R _g = 1 Ω		16		ns
Rise Time	t _r			14		
Turn-Off DelayTime	t _{d(off)}			60		
Fall Time	t _f			12		
Turn-On Delay Time	t _{d(on)}	V _{DS} = - 15 V, R _L = 1.5 Ω I _D ≅ - 15 A, V _{GS} = - 4.5 V, R _g = 1 Ω		60		
Rise Time	t _r			59		
Turn-Off DelayTime	t _{d(off)}			50		
Fall Time	t _f			22		
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 45	A
Pulse Diode Forward Current (100 μs)	I _{SM}				- 180	
Body Diode Voltage	V _{SD}	I _S = - 3 A, V _{GS} = 0		- 0.7	- 1.20	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 15 A, dI/dt = 100 A/μs, T _J = 25 °C		22		ns
Body Diode Reverse Recovery Charge	Q _{rr}			12		nC
Reverse Recovery Fall Time	t _a			9		ns
Reverse Recovery Rise Time	t _b			13		

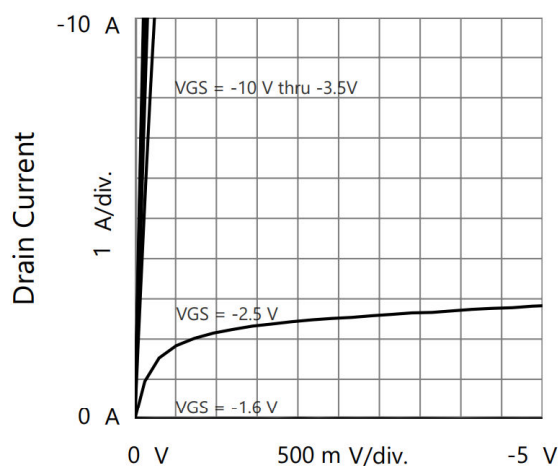
Notes:

 a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

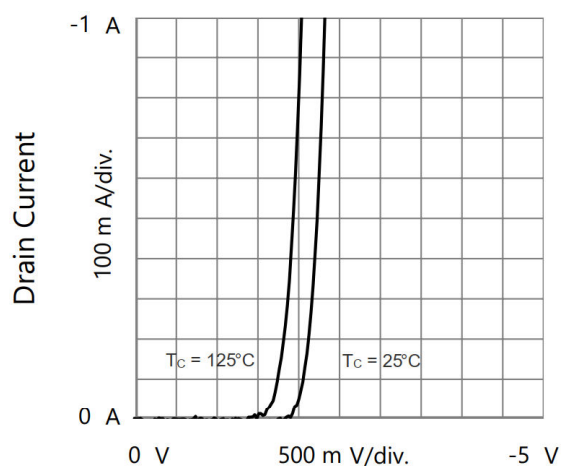
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

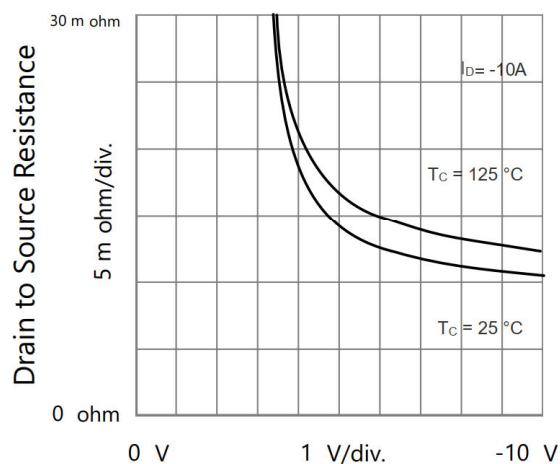
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



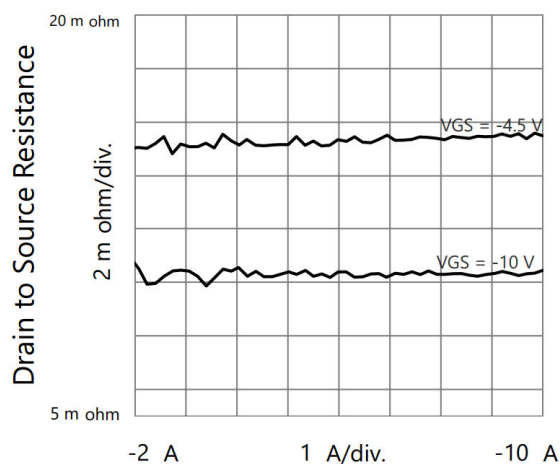
Drain to Source Voltage
Output Characteristics



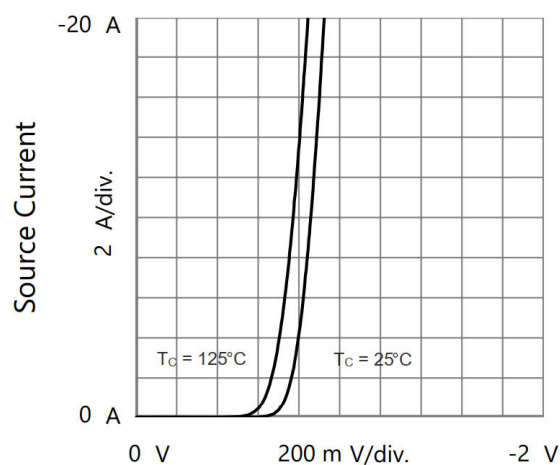
Gate to Source Voltage
Transfer Characteristics



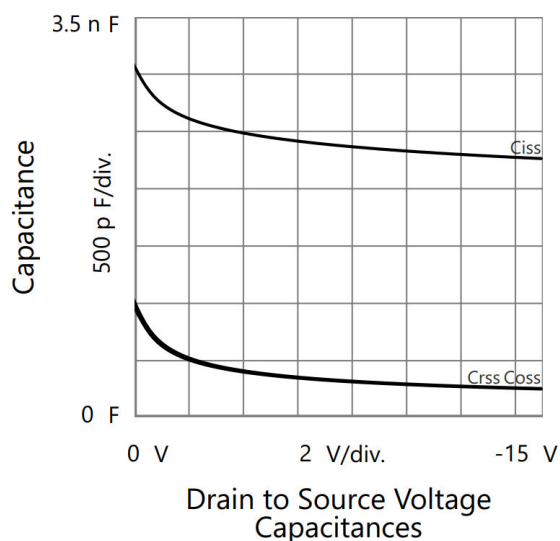
Gate to Source Voltage
Drain to Source Resistance vs. Gate to Source Voltage



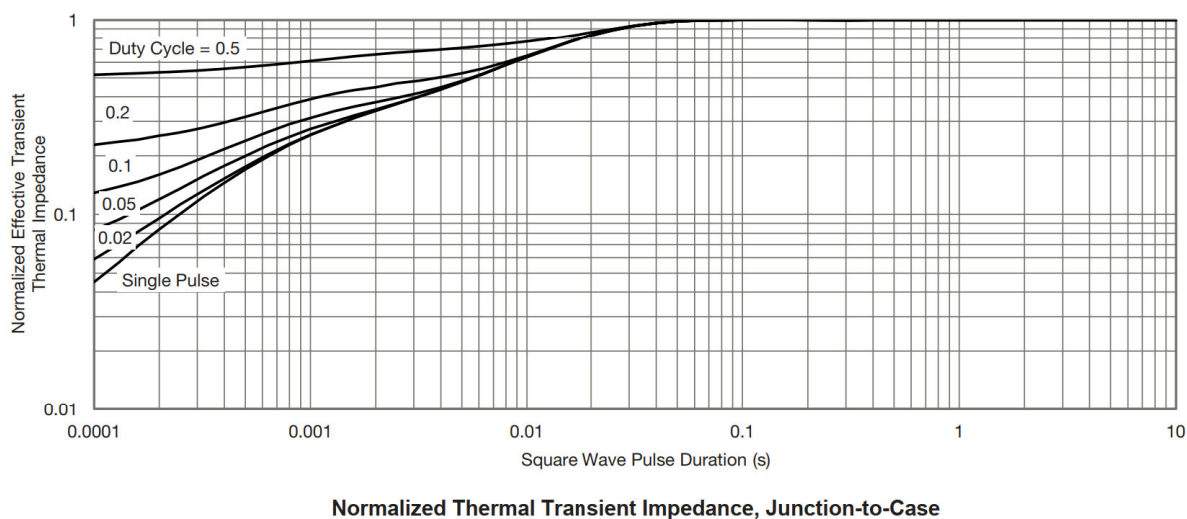
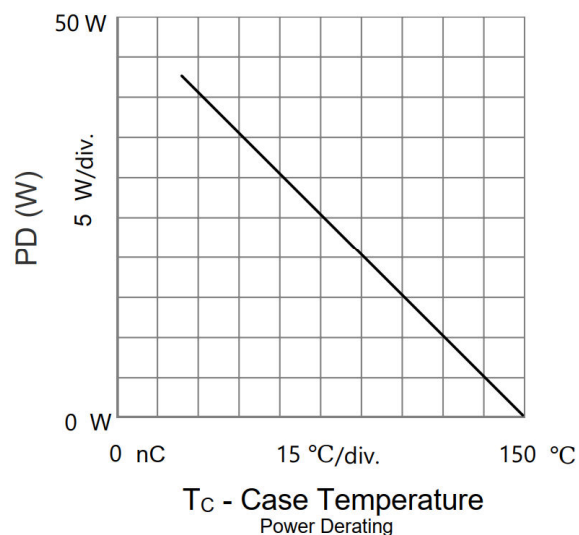
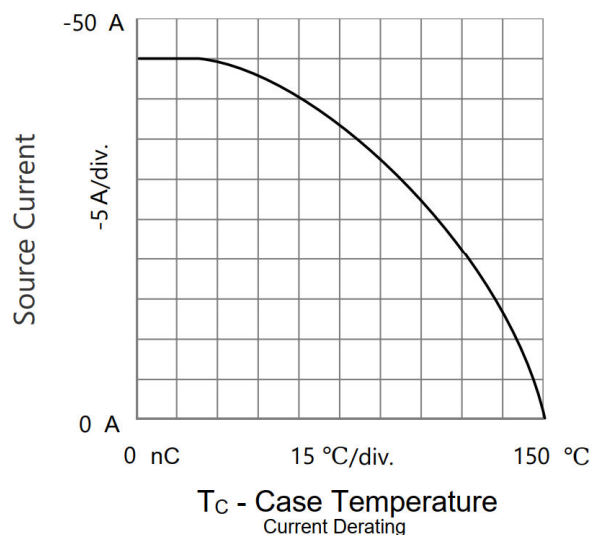
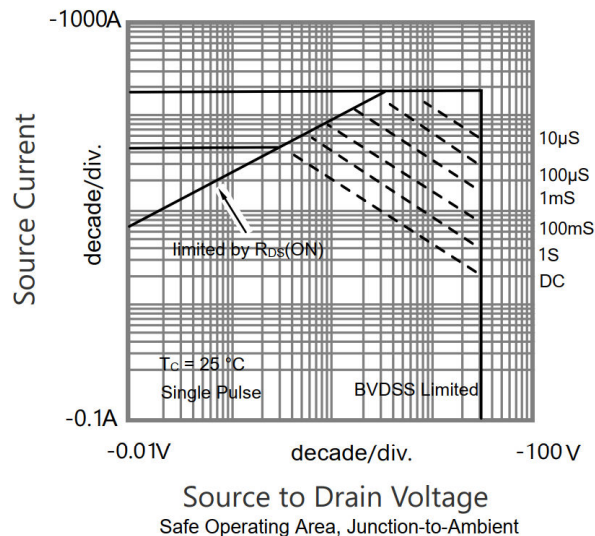
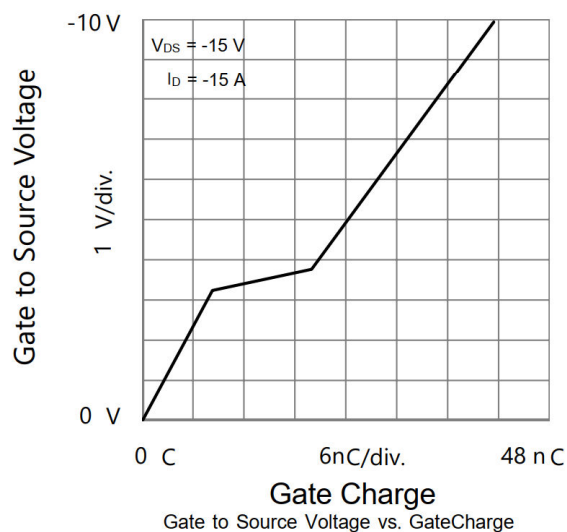
Drain Current
Drain to Source Resistance vs. Drain Current



Source to Drain Voltage
Body Diode Forward Characteristics



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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