P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (mΩ)(Typ.)	I_D (A)[a, e]	Q_g (Typ.)
-40	11 at V_{GS} = 10 V	-46[d]	47 nC
	16 at V_{GS} = 4.5 V		

FEATURES

- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested

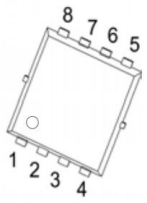
RoHS COMPLIANT

APPLICATIONS

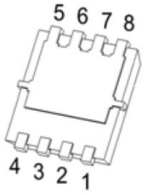
- Battery, Load and Adaptor Switches
  - Notebook Computers
  - Notebook Battery Packs

PDFN 3.3x3.3

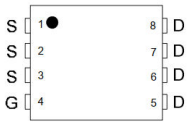
Top View

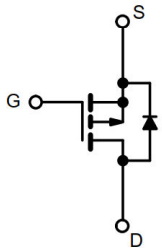


Bottom View



Top View





P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 46[d]	A
	T_C = 70 °C		- 35[d]	
	T_A = 25 °C		- 19[a, b]	
	T_A = 70 °C		- 14[a, b]	
Pulsed Drain Current (t = 100 µs)		I_{DM}	- 184	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 46[d]	
	T_A = 25 °C		- 3.8[a, b]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 42	
Single-Pulse Avalanche Energy		E_{AS}	79	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	79	W
	T_C = 70 °C		50.6	
	T_A = 25 °C		4.9[a, b]	
	T_A = 70 °C		3.1[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[e, f]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a, c]	t ≤ 10 s	R_{thJA}	20	26	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	1.3	1.6	

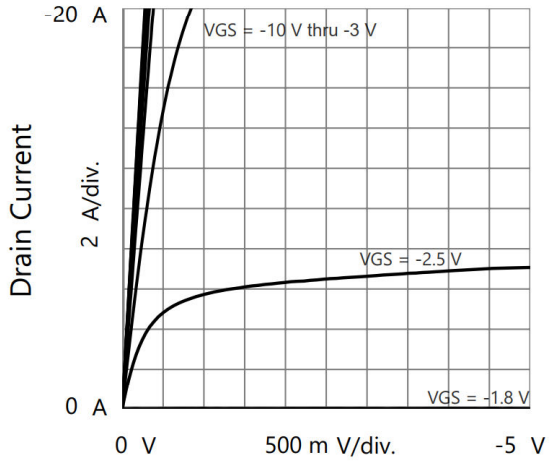
Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. Maximum under steady state conditions is 70 °C/W.
d. Package limited.
e. The DFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0, I_D = - 250 µA	- 40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 22		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			4.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1		- 3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 40 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 32 V, V_{GS} = 0 V, T_J = 55 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ - 10 V, V_{GS} = - 10 V	- 46			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 10 A		11	16	mΩ
		V_{GS} = - 4.5 V, I_D = - 5 A		16	22	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 10 A		45		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 20 V, V_{GS} = 0 V, f = 1 MHz		2730		pF
Output Capacitance	C_{oss}			215		
Reverse Transfer Capacitance	C_{rss}			204		
Total Gate Charge	Q_g	V_{DS} = - 20 V, V_{GS} = - 10 V, I_D = - 10 A		47		nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			13		
Gate Resistance	R_g	f = 1 MHz		3		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 20 V, R_L = 1.5 Ω $I_D \cong$ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω		29		ns
Rise Time	t_r			11		
Turn-Off DelayTime	$t_{d(off)}$			65		
Fall Time	t_f			10		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 20 V, R_L = 1.5 Ω $I_D \cong$ - 5 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		66		
Rise Time	t_r			57		
Turn-Off DelayTime	$t_{d(off)}$			49		
Fall Time	t_f			20		
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I_S	T_C = 25 °C			- 46	A
Pulse Diode Forward Current (100 µs)	I_{SM}				- 184	
Body Diode Voltage	V_{SD}	I_S = - 1 A		- 0.6	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 10 A, dI/dt = 100 A/µs, T_J = 25 °C		23	66	ns
Body Diode Reverse Recovery Charge	Q_{rr}			15	56	nC
Reverse Recovery Fall Time	t_a			9		ns
Reverse Recovery Rise Time	t_b			17		

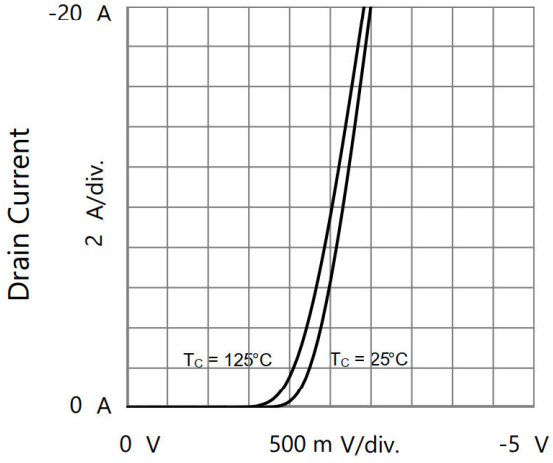
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operaticnal sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

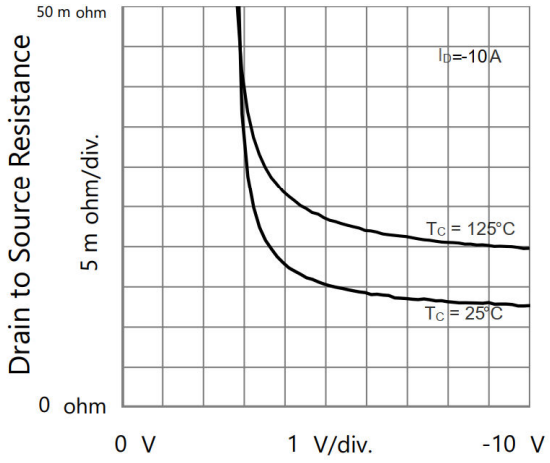
TYPICAL CHARACTERISTICS (25 C, unless otherwise noted)



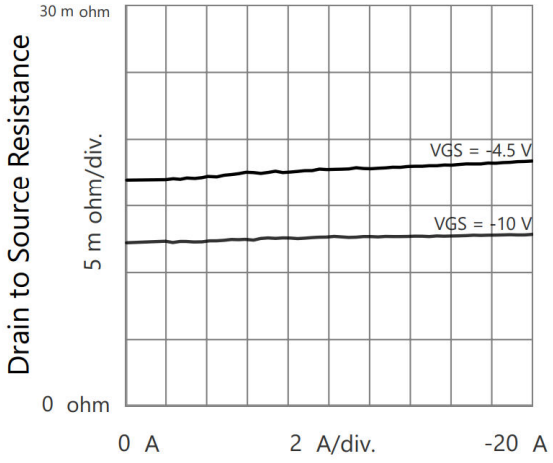
Drain to Source Voltage
Output Characteristics



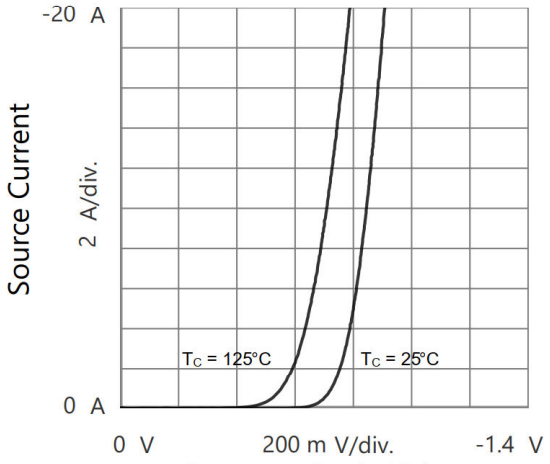
Gate to Source Voltage
Transfer Characteristics



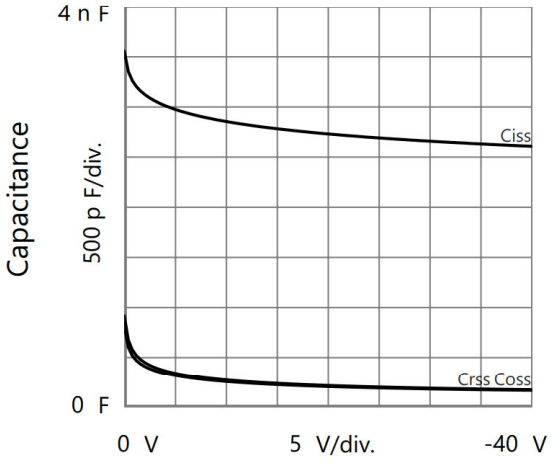
Gate to Source Voltage
Drain to Source Resistance vs. Gate to Source Voltage



Drain Current
Drain to Source Resistance vs. Drain Current

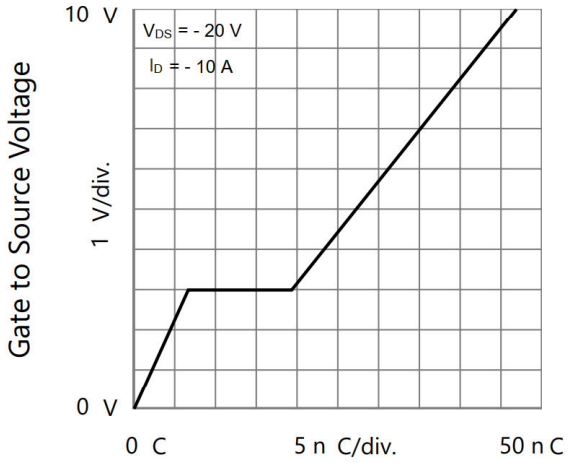


Source to Drain Voltage
Body Diode Forward Characteristics

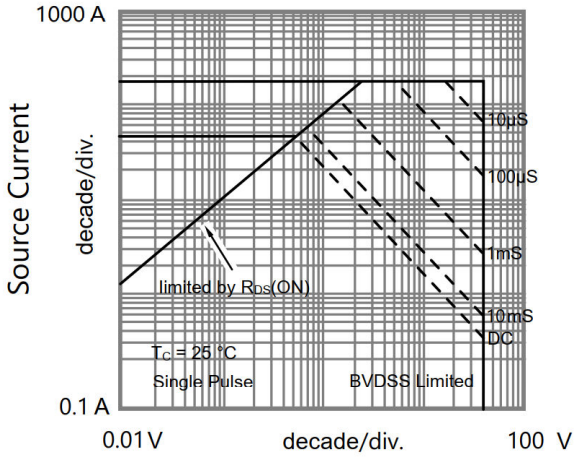


Drain to Source Voltage
Capacitances

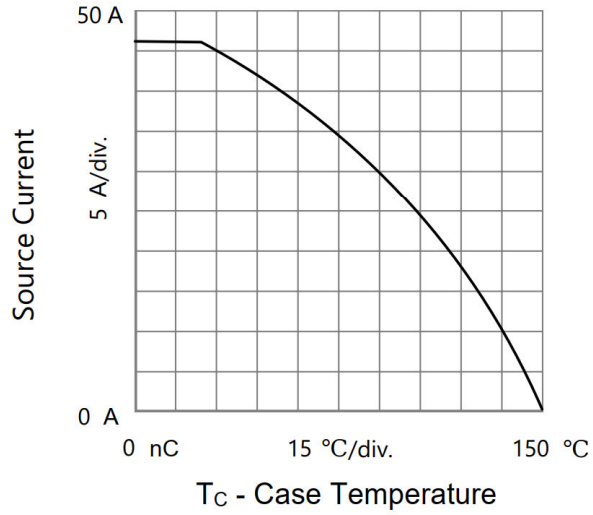
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

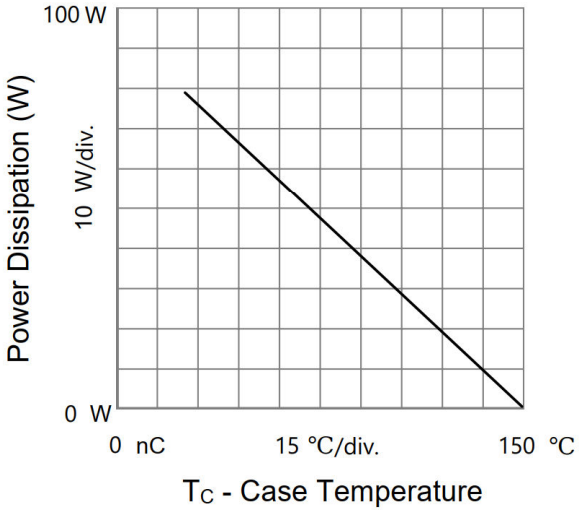


Gate to Source Voltage vs. GateCharge



Safe Operating Area, Junction-to-Ambient





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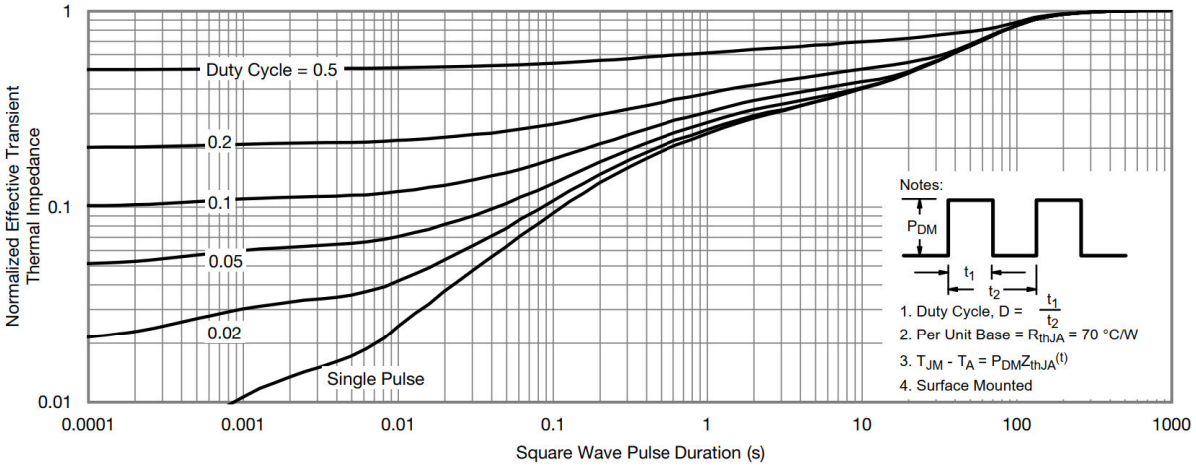
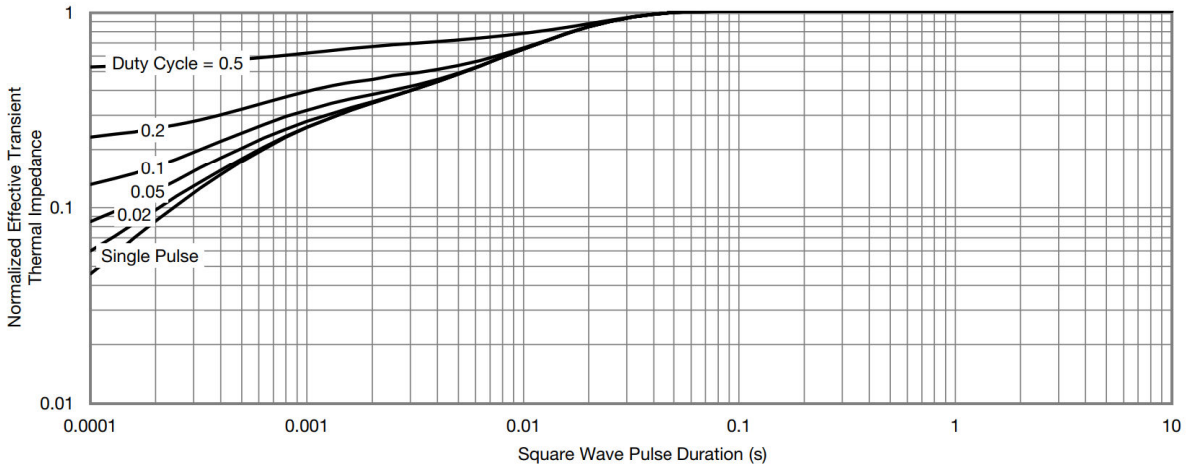


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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