

# N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ ) Max.	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)	
	0.0046 at V <sub>GS</sub> = 10 V	95		
100	0.0055 at V <sub>GS</sub> = 7.5 V	85	57.9 nC	
	0.0072 at V <sub>GS</sub> = 4.5 V	75		

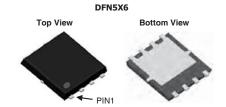
#### **FEATURES**

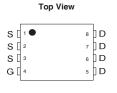
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 %  $\rm R_{\rm g}$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

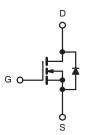


#### **APPLICATIONS**

- DC/DC Primary Side Switch
- Telecom/Server 48 V, Full/Half-Bridge DC/DC
- Industrial







N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b>	<b>S</b> (T <sub>A</sub> = 25 °C, unle	ess otherwise i	noted)		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	100	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20		
	T <sub>C</sub> = 25 °C		95		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	I <sub>D</sub>	86		
Continuous Brain Garrent (1) = 100 O)	T <sub>A</sub> = 25 °C		23.3 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C	1	20.6 <sup>b, c</sup>	А	
Pulsed Drain Current (t = 300 µs)		I <sub>DM</sub>	320	A	
Continuous Source-Drain Diode Current	$T_C = 25 ^{\circ}C$	S Is	95		
	T <sub>A</sub> = 25 °C	'S	7.5 <sup>b, c</sup>		
Single Pulse Avalanche Current L = 0.1 mH		I <sub>AS</sub>	90		
Single Pulse Avalanche Energy	L = 0.1 IIII1	E <sub>AS</sub>	300	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		145	W	
	T <sub>C</sub> = 70 °C	P <sub>D</sub>	93		
	T <sub>A</sub> = 25 °C	- 'D	8 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		5.1 <sup>b, c</sup>		
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>				260	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	20	25	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	2.1	2.8	] 0/1	

- a. Based on T<sub>C</sub> = 25 °C.
  b. Surface mounted on 1" x 1" FR4 board.
- d. The DFN5X6 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 70 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			ļ			!	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0$ , $I_D = 250 \mu A$	100			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		64		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	ι <sub>D</sub> = 250 μΑ		- 5.8			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.2		2.8	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Oata Waltana D. i. O i	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current		$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	95			Α	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.0046	0.006	<del>                                     </del>	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 12 A		0.0055	0.008	Ω	
		$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		0.0072	0.010		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A		11		S	
Dynamic <sup>b</sup>			L		l.	l	
Input Capacitance	C <sub>iss</sub>			4675		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		998			
Reverse Transfer Capacitance	C <sub>rss</sub>			58			
Total Gate Charge		V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		57.9	82		
	$Q_{g}$	$V_{DS} = 50 \text{ V}, V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$		51.6	73	1	
				43.9	61		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$		9.2		nC	
Gate-Drain Charge	$Q_{gd}$			19.3			
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		40	60		
Gate Resistance	$R_g$	f = 1 MHz	0.2	1.05	2.1	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			20	40		
Rise Time	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_L = 5 \Omega$		19	32		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		45	80		
Fall Time	t <sub>f</sub>			9	36		
Turn-On Delay Time	t <sub>d(on)</sub>			22	44	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_L = 5 \Omega$		21	36		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 10$ A, $V_{GEN}=7.5$ V, $R_g=1$ $\Omega$		48	85		
Fall Time	t <sub>f</sub>			11	46		
Drain-Source Body Diode Characteristic	s		•			'	
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			95	А	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				320	^	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 4 A		0.76	1.1	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			36	70	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 10 A, dl/dt = 100 A/µs, T <sub>.I</sub> = 25 °C		38	76	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	i <sub>F</sub> = 10 A, αί/αι = 100 A/μs, 1 <sub>J</sub> = 25 °C		22			
Reverse Recovery Rise Time	lecovery Rise Time t <sub>b</sub>			14		ns	

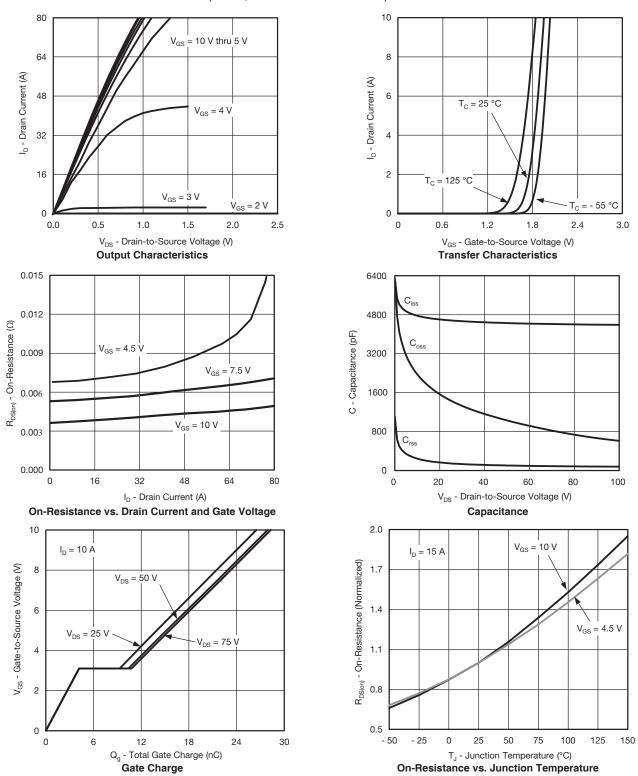
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.



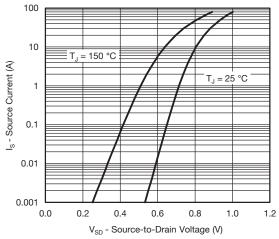
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## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

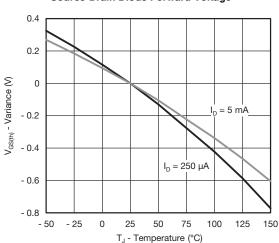




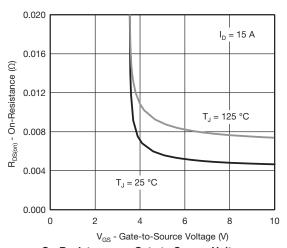
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



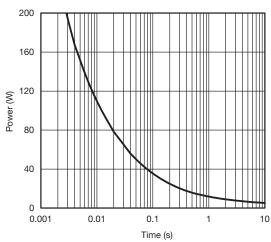
#### Source-Drain Diode Forward Voltage



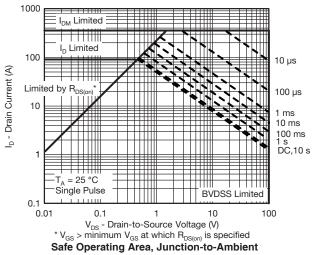
Threshold Voltage



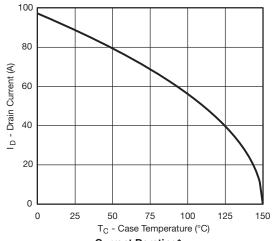
On-Resistance vs. Gate-to-Source Voltage



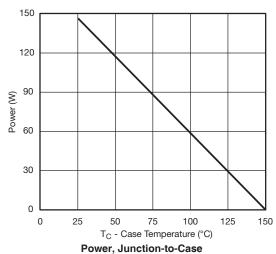
Single Pulse Power, Junction-to-Ambient

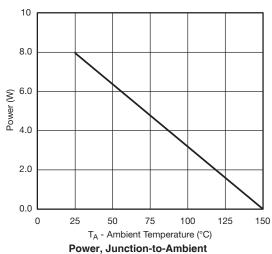


## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**Current Derating\*** 

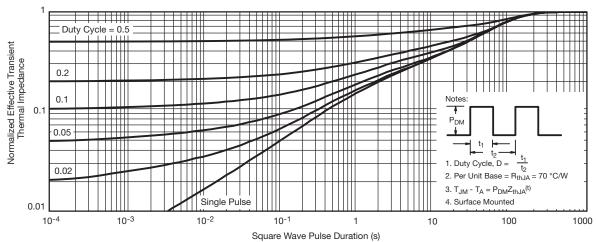




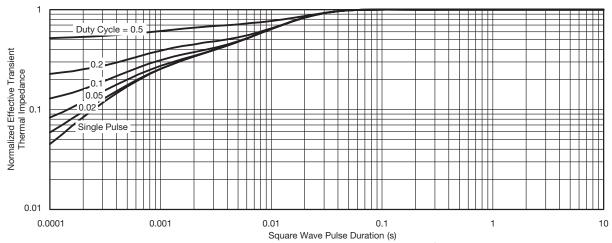
 $<sup>^{\</sup>star}$  The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150  $^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case





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