

## N-Channel 40 V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a, e</sup>	$Q_g$ (Typ.)
40	0.0012 at $V_{GS} = 10$ V	180	125 nC
	0.0016 at $V_{GS} = 4.5$ V	150	

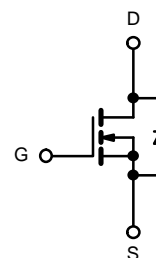
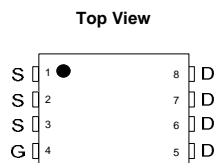
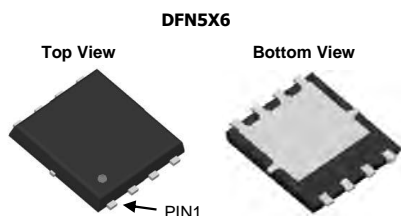
### FEATURES

- DT-Trench Power MOSFET
- 100 %  $R_g$  and UIS Tested


**RoHS**  
 COMPLIANT

### APPLICATIONS

- Notebook PC Core
- VRM/POL



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C)	$T_C = 25$ °C	$I_D$	A
	$T_C = 70$ °C		
	$T_A = 25$ °C		
	$T_A = 70$ °C		
Pulsed Drain Current	$I_{DM}$	420	mJ
Avalanche Current Pulse	$I_{AS}$	46	
Single Pulse Avalanche Energy	$E_{AS}$	580	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	$I_S$	A
	$T_A = 25$ °C		
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	W
	$T_C = 70$ °C		
	$T_A = 25$ °C		
	$T_A = 70$ °C		
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	$R_{thJA}$	14	18	°C/W
Maximum Junction-to-Case	$R_{thJC}$	0.45	0.7	

Notes:

 a. Based on  $T_C = 25$  °C.

b. Surface mounted on 1" x 1" FR4 board.

 c.  $t = 10$  s.

d. Maximum under steady state conditions is 90 °C/W.

e. Calculated based on maximum junction temperature. Package limitation current is 80 A.

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min .	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		40		V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		35		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 5.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1		3	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	180			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		0.0012	0.0015	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		0.0015	0.0019	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		80		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		5885		pF
Output Capacitance	C <sub>oss</sub>			3842		
Reverse Transfer Capacitance	C <sub>rss</sub>			160		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		125		nC
		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		57.3		
Gate-Source Charge	Q <sub>gs</sub>			18		
Gate-Drain Charge	Q <sub>gd</sub>			13		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.555 Ω I <sub>D</sub> ≅ 30A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		14	22	ns
Rise Time	t <sub>r</sub>			10	16	
Turn-Off Delay Time	t <sub>d(off)</sub>			56	85	
Fall Time	t <sub>f</sub>			10	15	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.625 Ω I <sub>D</sub> ≅ 20 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		12	20	
Rise Time	t <sub>r</sub>			150	220	
Turn-Off Delay Time	t <sub>d(off)</sub>			55	83	
Fall Time	t <sub>f</sub>			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			180	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				420	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 22 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		35	58	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			90.2	125	nC
Reverse Recovery Fall Time	t <sub>a</sub>			27		ns
Reverse Recovery Rise Time	t <sub>b</sub>			25		

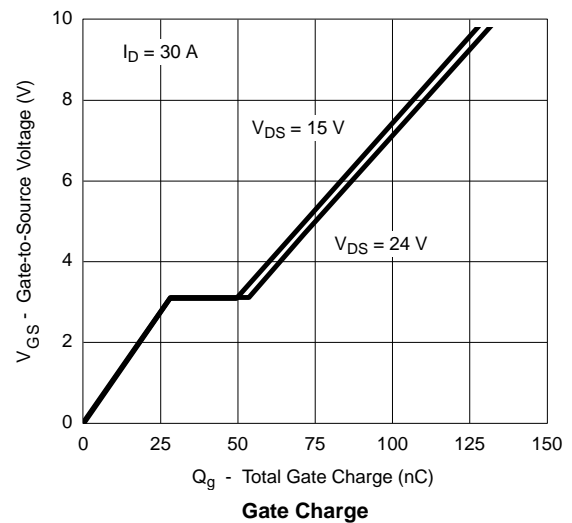
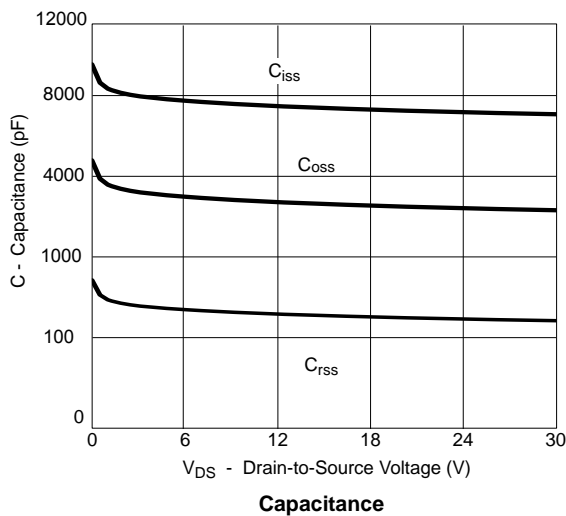
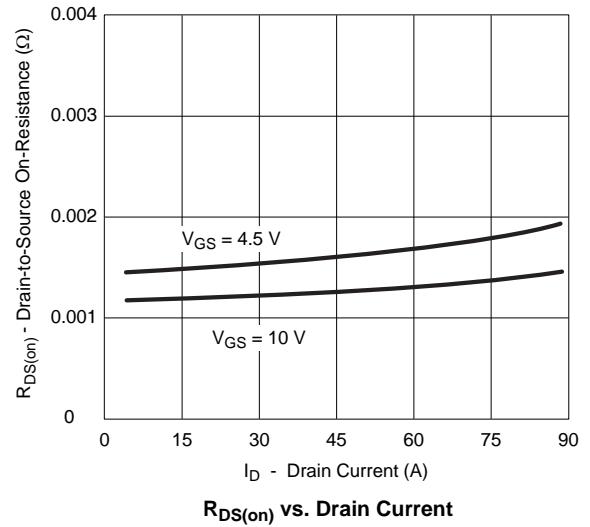
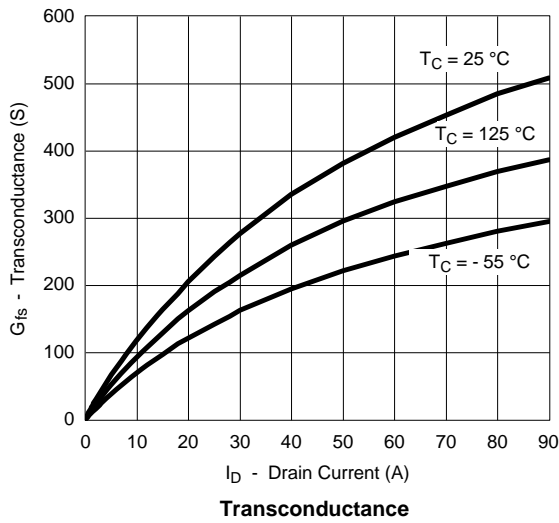
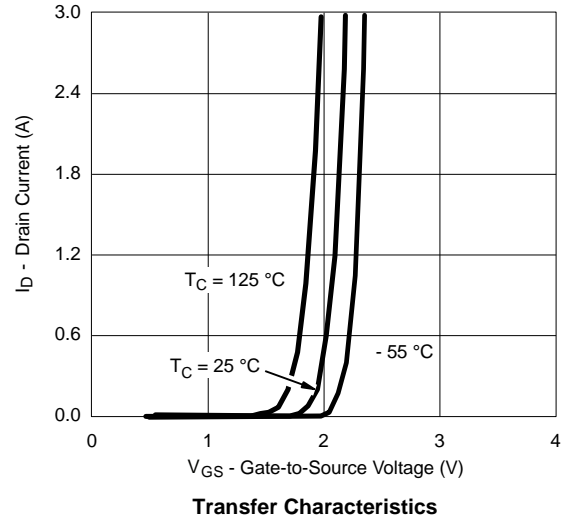
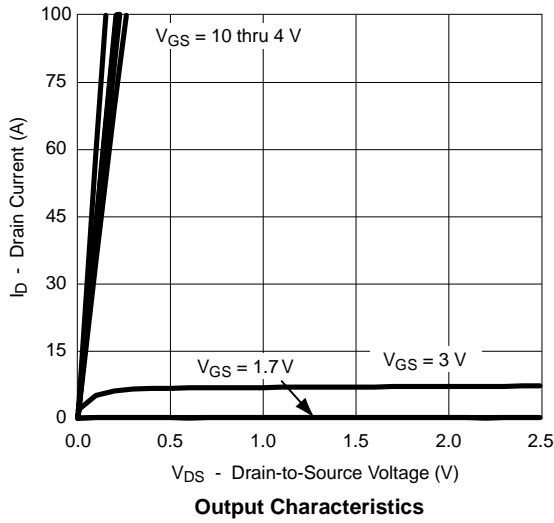
Notes:

 a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

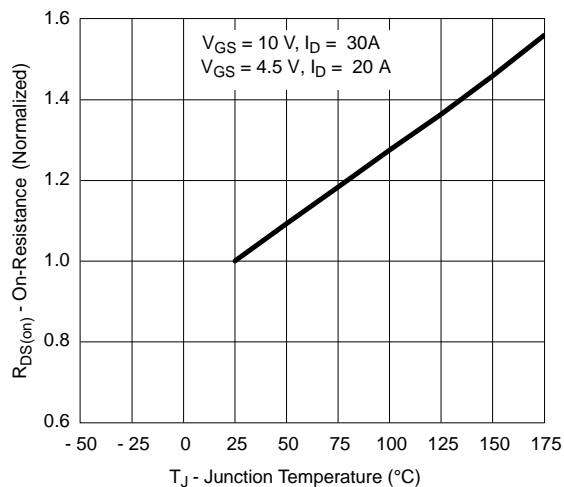
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

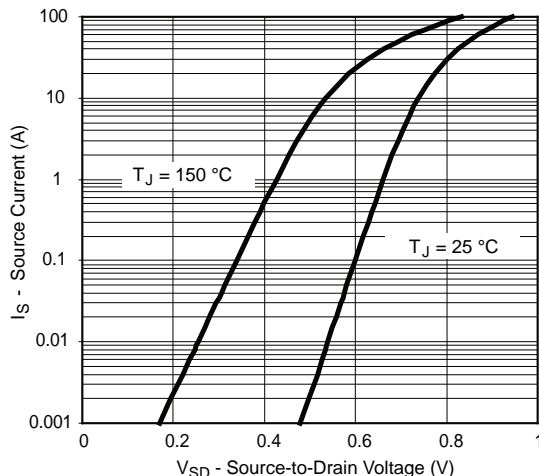
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



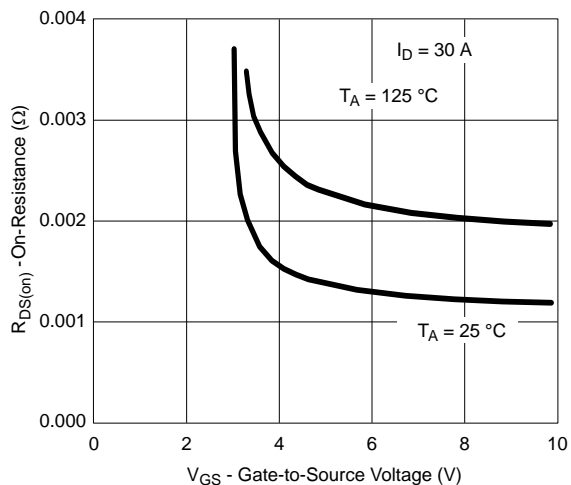
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



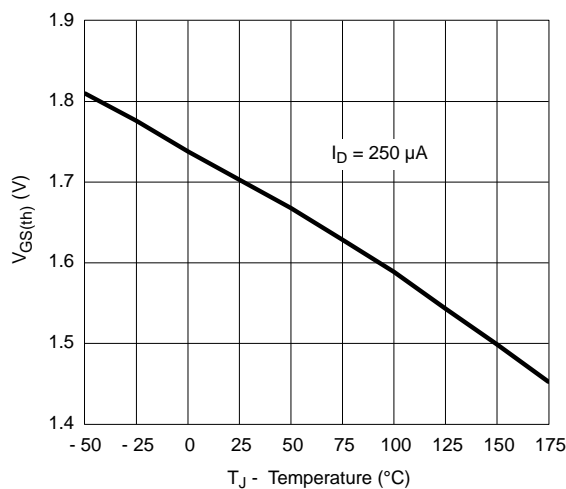
**On-Resistance vs. Junction Temperature**



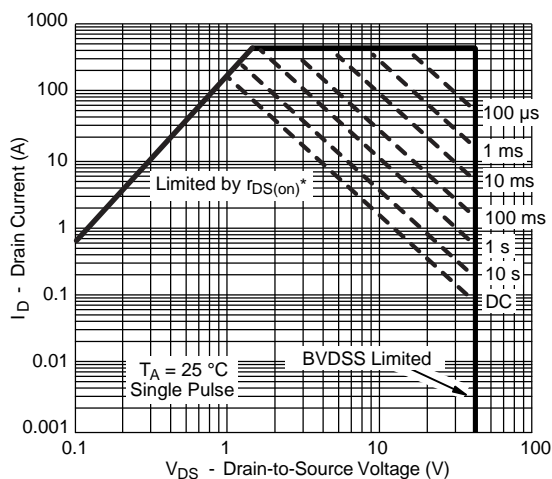
**Forward Diode Voltage vs. Temperature**



**$R_{DS(on)}$  vs.  $V_{GS}$  vs. Temperature**



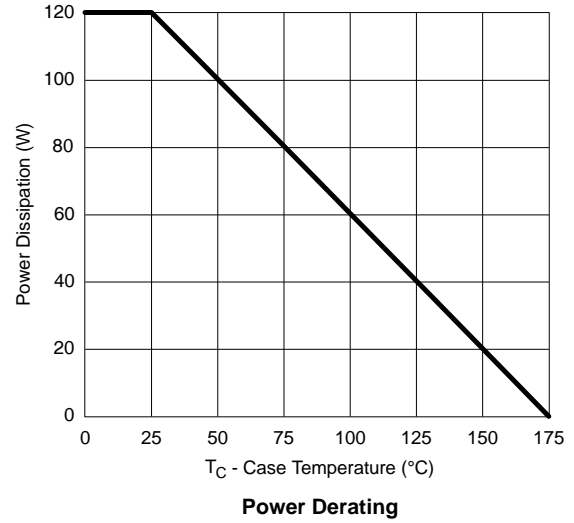
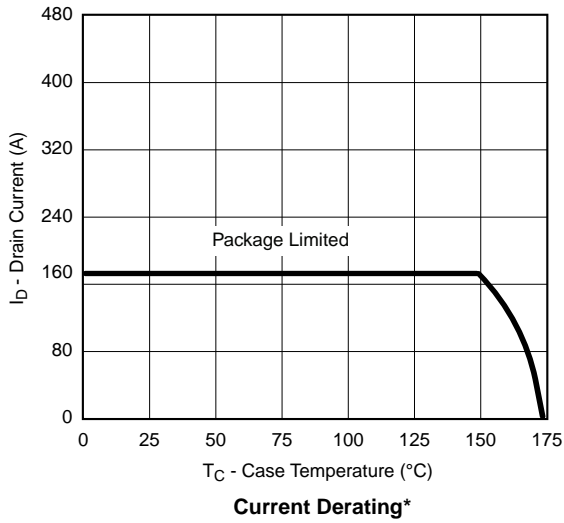
**Threshold Voltage**



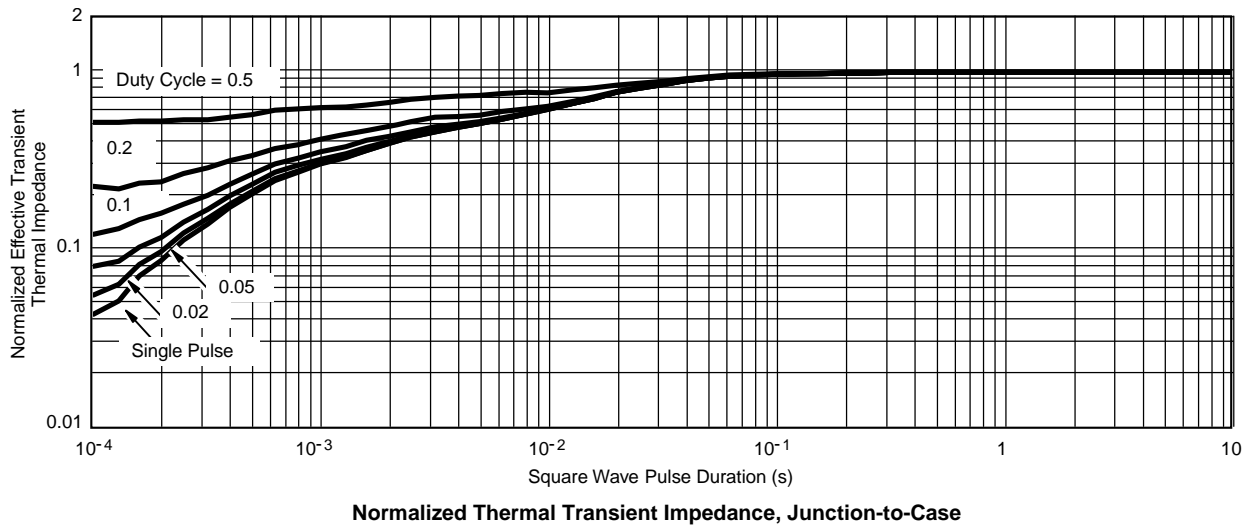
\* $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



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