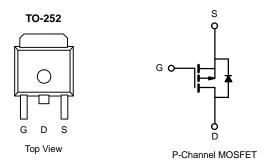


P-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	R _{DS(on)} (Ω) I _D (A)		Q _g (Typ.)	
- 100	0.450 at V _{GS} = - 10 V	- 10	29 nC	
	0.560 at V_{GS} = - 4.5 V	- 7.3	29110	



FEATURES

- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Active Clamp in Intermediate DC/DC Power Supplies
- H-Bridge High Side Switch for Lighting Application



ABSOLUTE MAXIMUM RATINGS (T _A =	25 C, uniess ou	leiwise noteu)			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	- 100	V		
Gate-Source Voltage		V _{GS}	± 20		
	T _C = 25 °C		- 10		
Continuous Drain Current (T 150 °C)	T _C = 70 °C		- 9.2		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	- 1.3 ^{a, b}		
	T _A = 70 °C		- 1.1 ^{a, b}	A	
Pulsed Drain Current		I _{DM}	- 36		
Continuous Source Drain Diada Current	T _C = 25 °C	1.	- 10		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 1.3 ^{a, b}		
Avalanche Current	L = 0.1 mH	I _{AS}	- 9.8		
Single-Pulse Avalanche Energy		E _{AS}	83	mJ	
	T _C = 25 °C		33		
Maximum Bawer Dissingtion	T _C = 70 °C	P _D	21	w	
Maximum Power Dissipation	T _A = 25 °C	'D	3.2 ^{a, b}	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	
	T _A = 70 °C		1.9 ^{a, b}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 50 to 150	℃	
Soldering Recommendations (Peak Temperature)			260	·C	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.



THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, b}	t ≤ 10 s	R _{thJA}	40	60	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.9	2.5		

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 81 °C/W.

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 100			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = - 250 μA		- 165			
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	i _D = - 250 μA		- 6.6		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 1		- 3	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zara Cata Valtaga Drain Current	I _{DSS}	$V_{DS} = -100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-		- 1		
Zero Gate Voltage Drain Current		V_{DS} = - 100 V, V_{GS} = 0 V, T_{J} = 55 °C			- 10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -5 V$, $V_{GS} = -10 V$	- 15			Α	
	P	V _{GS} = - 10 V, I _D = - 3 A		0.450	0.550	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 6 V, I _D = - 2 A		0.560	0.700	52	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = 3 A		15		S	
Dynamic ^b							
Input Capacitance	C _{iss}			458		pF	
Output Capacitance	C _{oss}	$V_{DS} = -50 V$, $V_{GS} = 0 V$, f = 1 MHz		69			
Reverse Transfer Capacitance	C _{rss}			22			
Total Gate Charge	Qg	Q _g		29			
Gate-Source Charge	Q _{gs}	V_{DS} = - 75 V, V_{GS} = - 10 V, I_{D} = - 3 A		3.9		nC	
Gate-Drain Charge	Q _{gd}			8.1			
Gate Resistance	R _g	f = 1 MHz		6.0		Ω	
Turn-On Delay Time	t _{d(on)}			25			
Rise Time	t _r	V_{DD} = - 75 V, R_L = 25 Ω		85			
Turn-Off DelayTime	t _{d(off)}	${ m I}_{ m D}\cong$ - 2 A, ${ m V}_{ m GEN}$ = - 4.5 V, ${ m R}_{ m g}$ = 1 Ω		68			
Fall Time	t _f			44			
Turn-On Delay Time	t _{d(on)}			11		ns	
Rise Time	tr	V_{DD} = - 75 V, R_L = 25 Ω		48			
Turn-Off DelayTime	t _{d(off)}	$I_{D}\cong$ - 3 A, V_{GEN} = - 10 V, R_{g} = 1 Ω		32		-	
Fall Time	t _f			35			
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			- 10	А	
Pulse Diode Forward Current ^a	I _{SM}				- 36	~	
Body Diode Voltage	V _{SD}	I _S = - 3 A		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			45		ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = - 3 A, dl/dt = 100 A/μs, T _J = 25 °C		70		nC	
Reverse Recovery Fall Time	t _a	$F = -3 A$, $u/ut = 100 A/\mu s$, $T_{\rm J} = 25 C$		45			
Reverse Recovery Rise Time	t _b	1		20		ns	

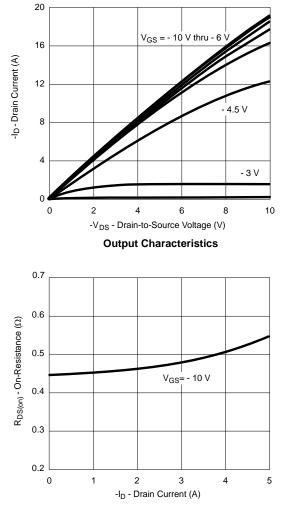
Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

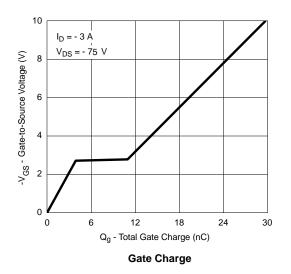
b. Guaranteed by design, not subject to production testing.

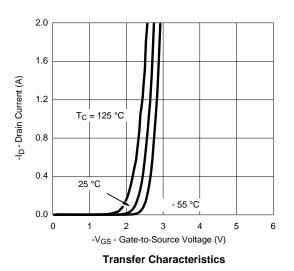
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

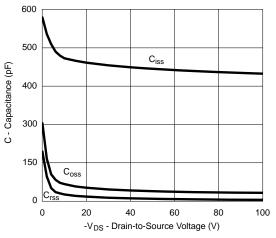




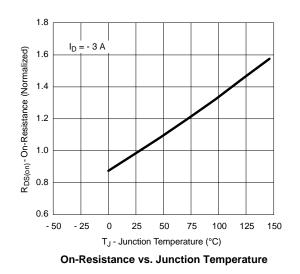
On-Resistance vs. Drain Current and Gate Voltage



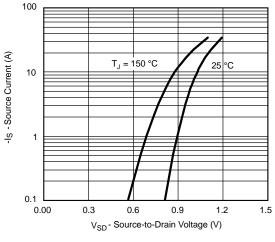




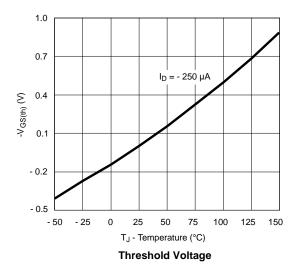


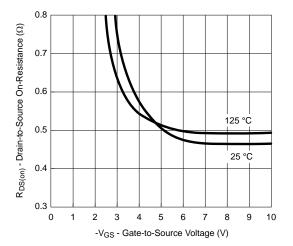




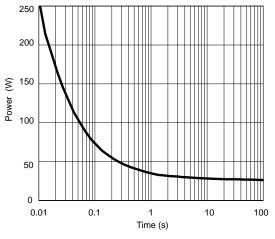


Source-Drain Diode Forward Voltage

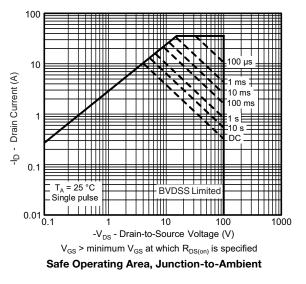




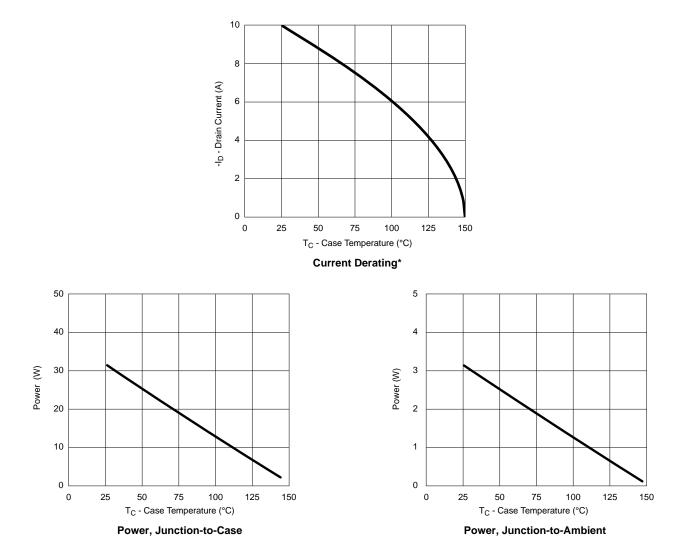
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

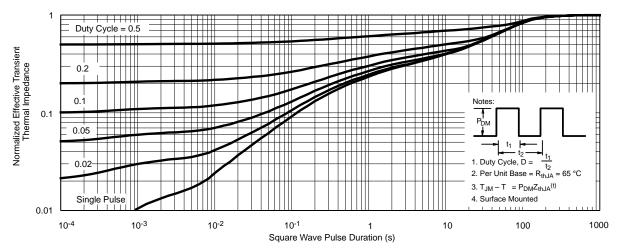


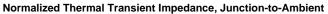


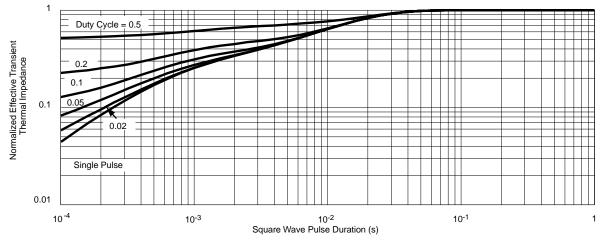


* The power dissipation PD is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.









Normalized Thermal Transient Impedance, Junction-to-Foot



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