

N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{a, e}	Q_g (Typ.)
40	0.015 at $V_{GS} = 10$ V	28	17 nC
	0.017 at $V_{GS} = 4.5$ V	25	

FEATURES

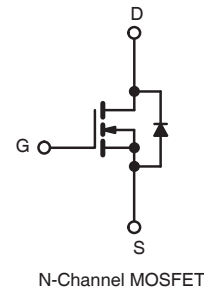
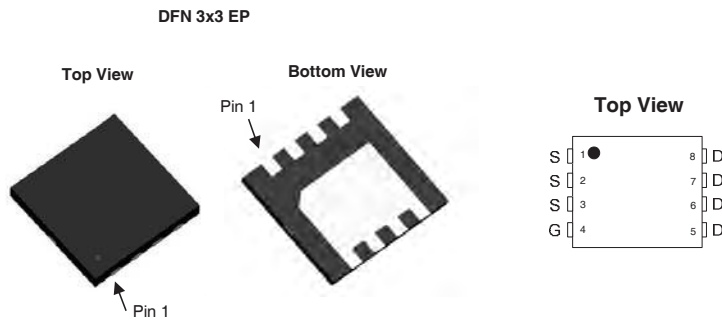
- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested

APPLICATIONS

- Notebook PC Core
- VRM/POL



RoHS
COMPLIANT



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	$T_C = 25$ °C	28 ^{a, e}
		$T_C = 70$ °C	22 ^e
		$T_A = 25$ °C	10 ^{b, c}
		$T_A = 70$ °C	8 ^{b, c}
Pulsed Drain Current	I_{DM}	112	mJ
Avalanche Current Pulse	I_{AS}	29	
Single Pulse Avalanche Energy	E_{AS}	43	
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	28 ^{a, e}
		$T_A = 25$ °C	12 ^{b, c}
Maximum Power Dissipation	P_D	$T_C = 25$ °C	25
		$T_C = 70$ °C	17
		$T_A = 25$ °C	2.9 ^{b, c}
		$T_A = 70$ °C	1.4 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	35	55	°C/W
Maximum Junction-to-Case	R_{thJC}	4	5	

Notes:

- Based on $T_C = 25$ °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under steady state conditions is 90 °C/W.
- Calculated based on maximum junction temperature. Package limitation current is 10 A.

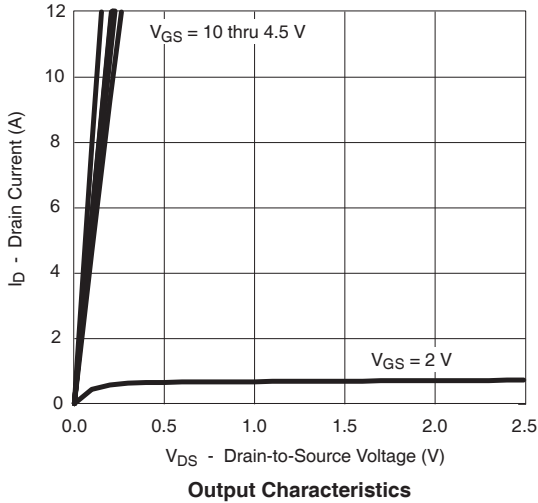
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	28			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		0.015	0.018	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		0.017	0.022	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 32\text{ V}, I_D = 10\text{ A}$		90		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1810		μF
Output Capacitance	C_{oss}			920		
Reverse Transfer Capacitance	C_{rss}			245		
Total Gate Charge	Q_g	$V_{DS} = 32\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		17		nC
		$V_{DS} = 32\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		10		
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			3		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.5	2.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 32\text{ V}, R_L = 0.555\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		16		ns
Rise Time	t_r			11		
Turn-Off Delay Time	$t_{d(off)}$			32		
Fall Time	t_f			8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 32\text{ V}, R_L = 0.625\text{ }\Omega$ $I_D \cong 8\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		36		
Rise Time	t_r			59		
Turn-Off Delay Time	$t_{d(off)}$			23		
Fall Time	t_f			8		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			28	A
Pulse Diode Forward Current ^a	I_{SM}				112	
Body Diode Voltage	V_{SD}	$I_S = 12\text{ A}$		0.7	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		50	71	ns
Body Diode Reverse Recovery Charge	Q_{rr}			65	94	nC
Reverse Recovery Fall Time	t_a			23		ns
Reverse Recovery Rise Time	t_b			20		

Notes:

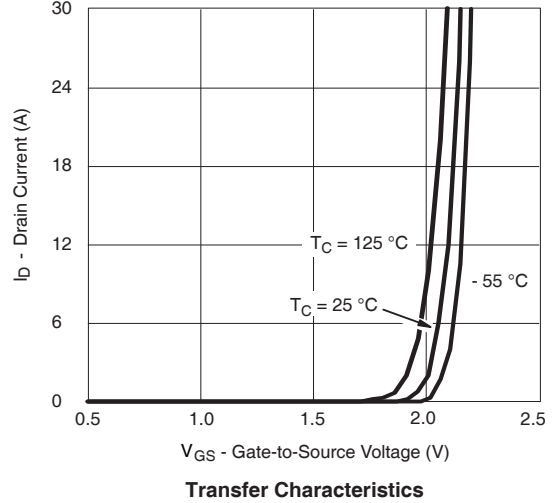
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

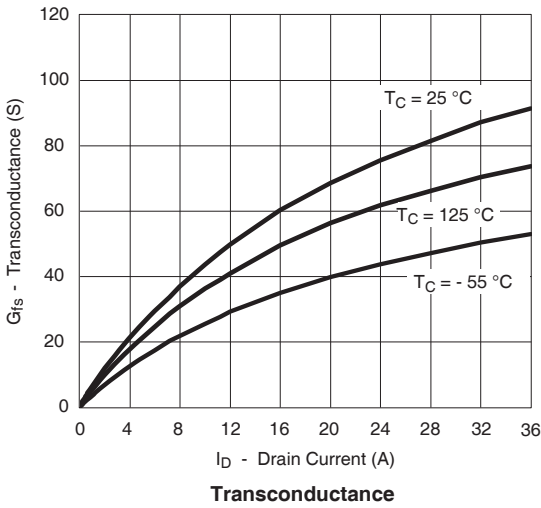
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



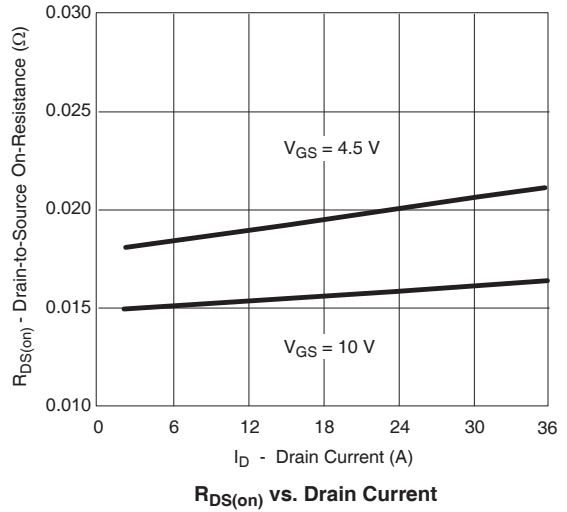
Output Characteristics



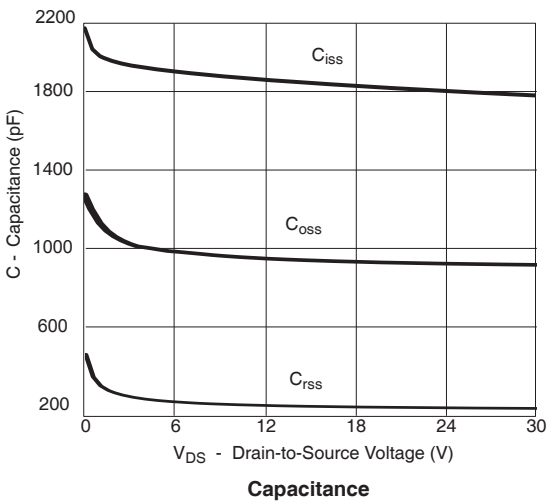
Transfer Characteristics



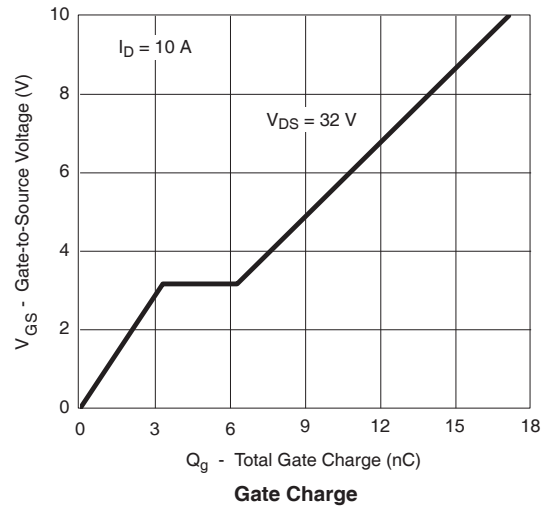
Transconductance



$R_{DS(on)}$ vs. Drain Current

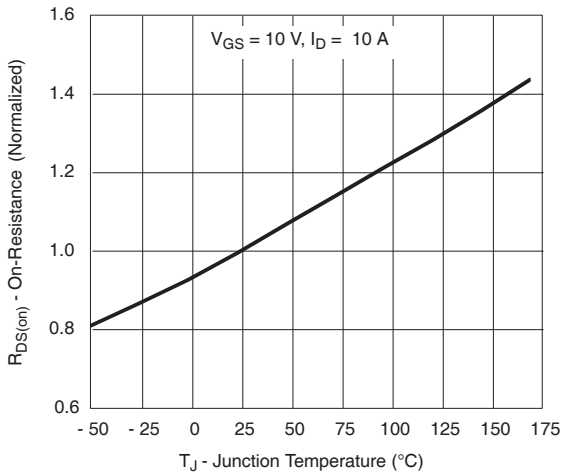


Capacitance

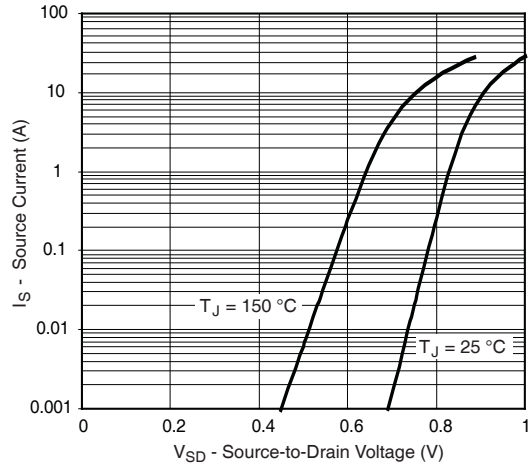


Gate Charge

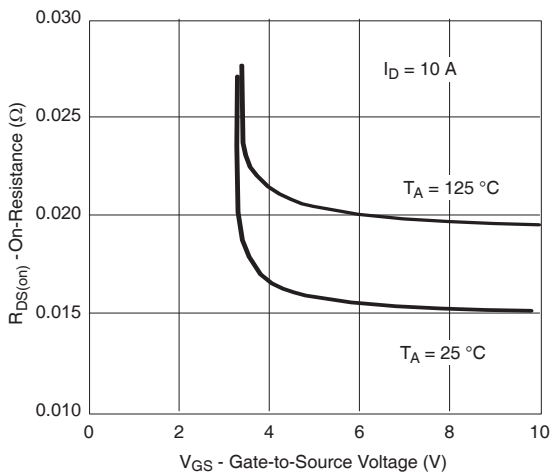
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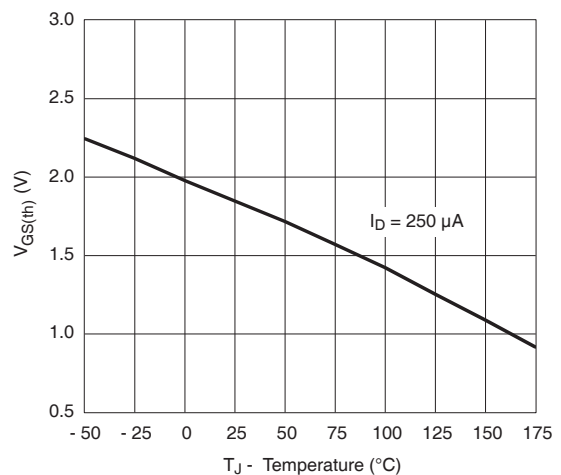
On-Resistance vs. Junction Temperature



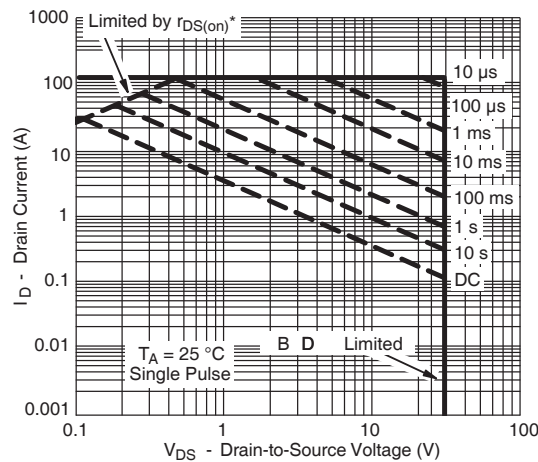
Forward Diode Voltage vs. Temperature



R_{DS(on)} vs. V_{GS} vs. Temperature

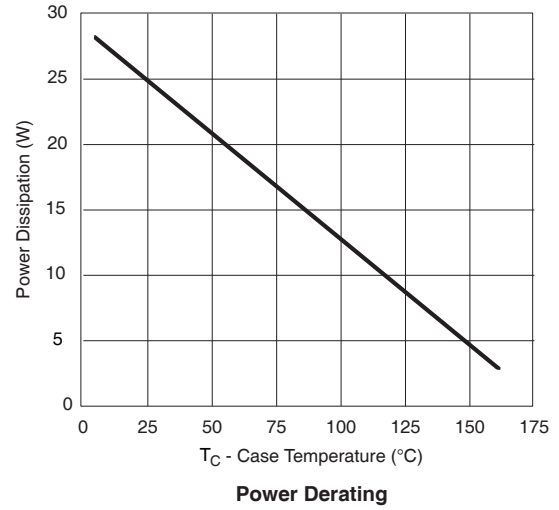
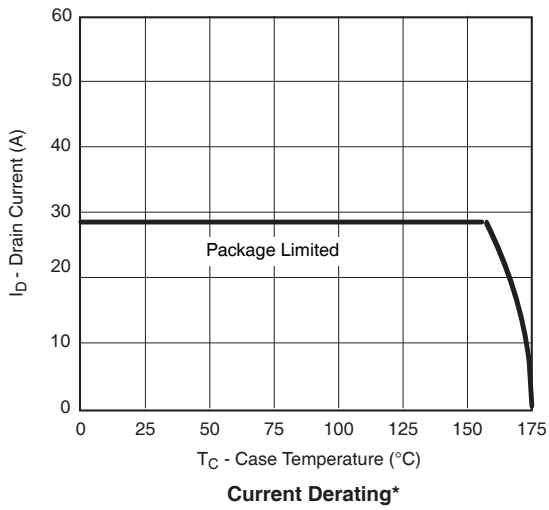


Threshold Voltage

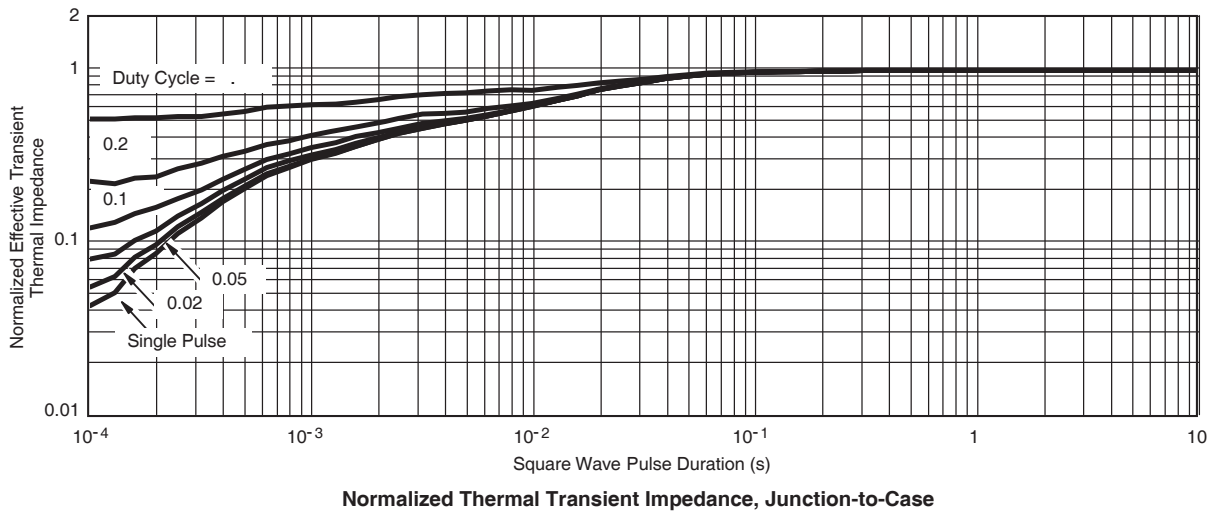


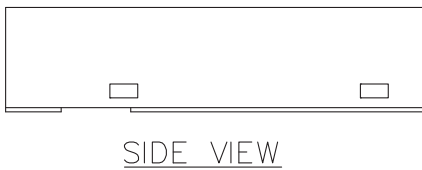
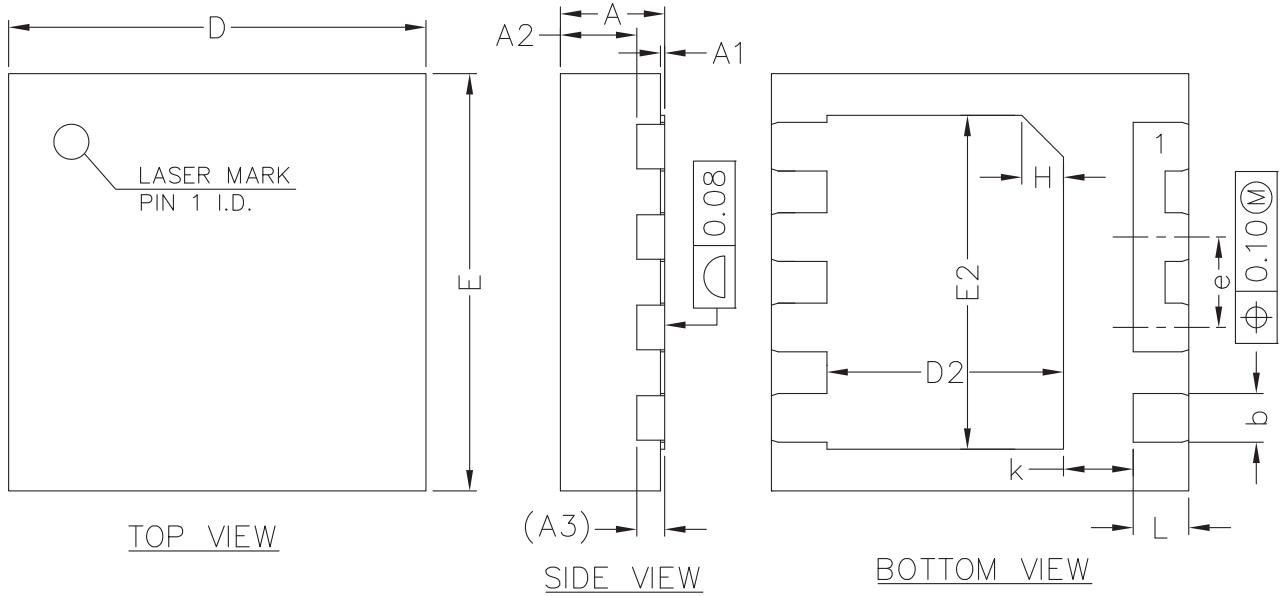
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



* The power dissipation P_D is based on $T_{J(max)} = 175\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.30	0.35	0.40
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.60	1.70	1.80
E2	2.30	2.40	2.50
e	0.55	0.65	0.75
K	0.40	0.50	0.60
L	0.35	0.40	0.45

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