

N-Channel 100 V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (mΩ)(Typ.)	I _D (A)(Max.)
100	7.8 at V _{GS} = 10 V	70 ^a

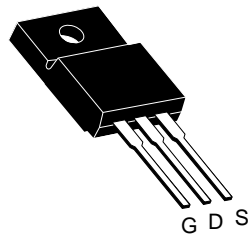
FEATURES

- Super Junction MOSFET
- New Package with Low Thermal Resistance
- 100 % R_g Tested

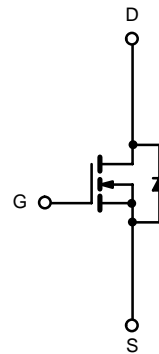


RoHS
COMPLIANT

TO-220 FULLPAK



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 175 °C)	I _D	T _C = 25 °C	70 ^a
		T _C = 125 °C	51 ^a
Pulsed Drain Current	I _{DM}	225	A
Avalanche Current	I _{AR}	55	
Repetitive Avalanche Energy ^b	E _{AR}	160	mJ
Maximum Power Dissipation ^b	P _D	T _C = 25 °C	78 ^c
		T _A = 25 °C	2.15
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R _{thJA}	55	°C/W
Junction-to-Case (Drain)	R _{thJC}	4	

Notes:

- Package limited.
- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

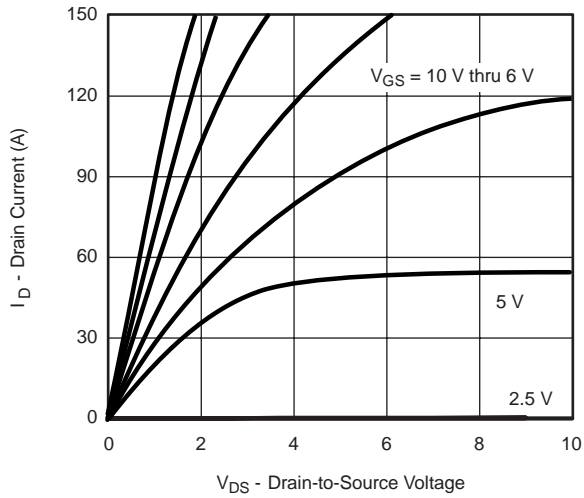
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		7.8	8.5	m Ω
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125\text{ }^\circ\text{C}$		9	13	
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 175\text{ }^\circ\text{C}$		14	20	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$	25			S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		3300		μF
Output Capacitance	C_{oss}			350		
Reverse Transfer Capacitance	C_{rss}			22		
Total Gate Charge ^c	Q_g	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		40		nC
Gate-Source Charge ^c	Q_{gs}			14		
Gate-Drain Charge ^c	Q_{gd}			6		
Gate Resistance	R_g			0.6		Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 0.6\text{ }\Omega$ $I_D \cong 30\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$		19		ns
Rise Time ^c	t_r			12		
Turn-Off Delay Time ^c	$t_{d(off)}$			35		
Fall Time ^c	t_f			8		
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}$ ^b						
Continuous Current	I_S				70	A
Pulsed Current	I_{SM}				225	
Forward Voltage ^a	V_{SD}	$I_F = 30\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 30\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		40		ns
Peak Reverse Recovery Charge	$I_{RM(REC)}$			5.5		A
Reverse Recovery Charge	Q_{rr}			190		nC

Notes:

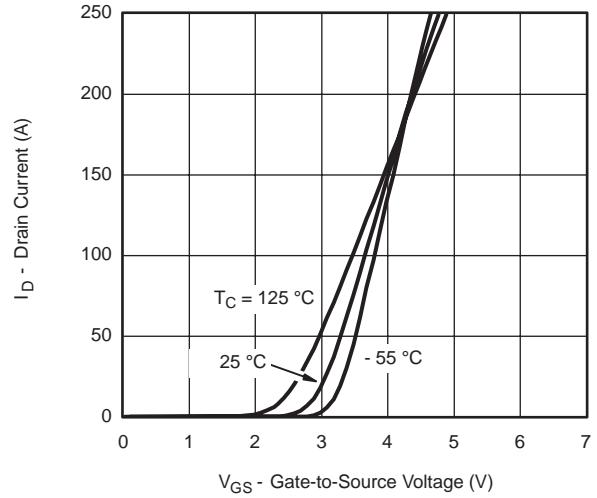
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

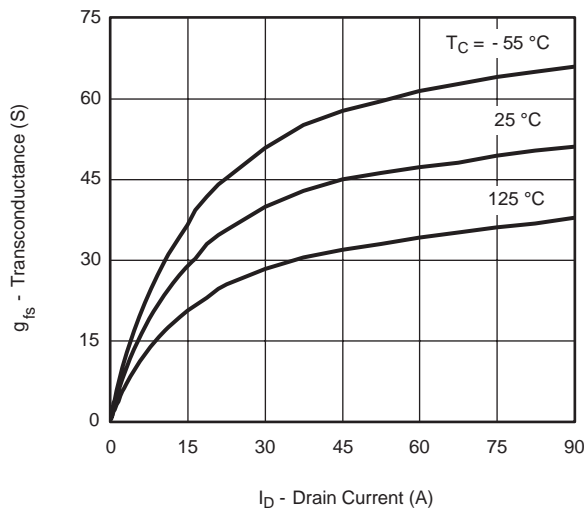
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



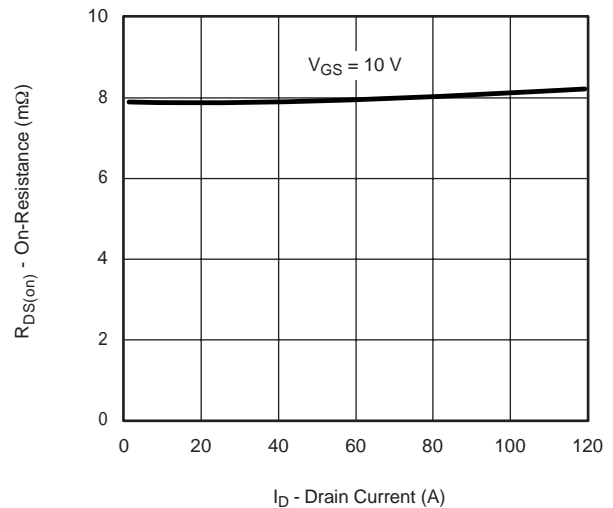
Output Characteristics



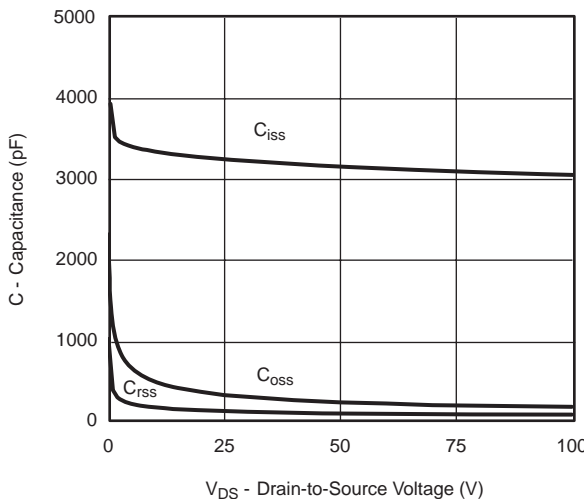
Transfer Characteristics



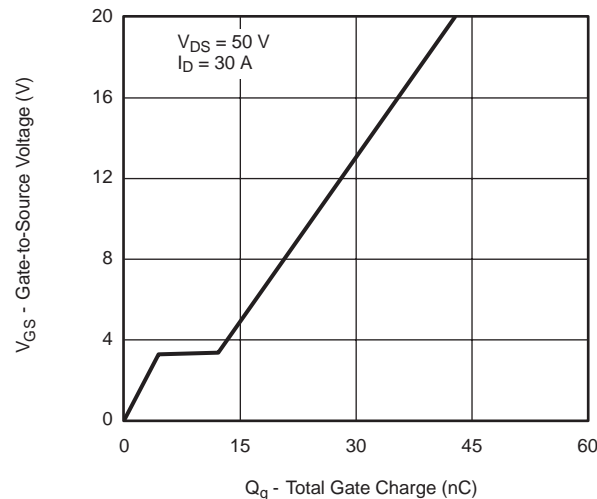
Transconductance



On-Resistance vs. Drain Current

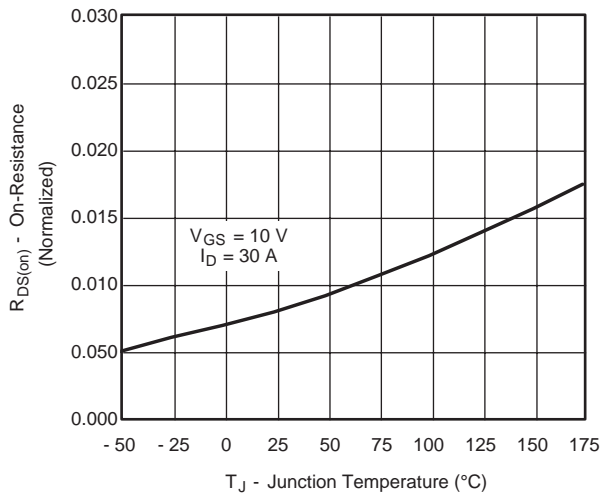


Capacitance

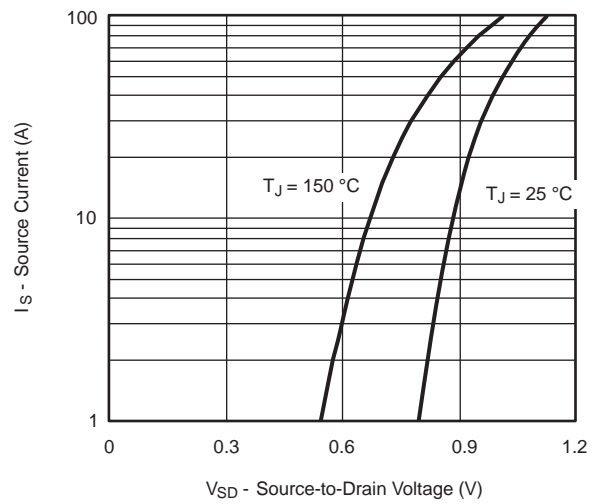


Gate Charge

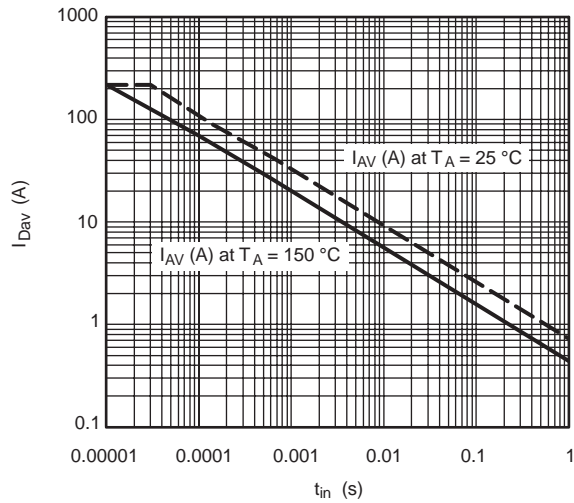
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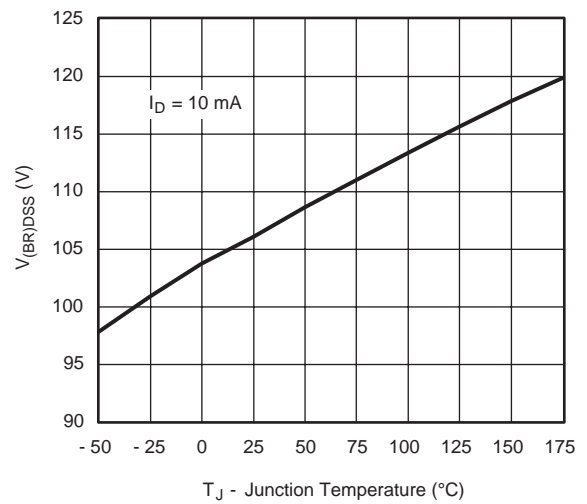
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

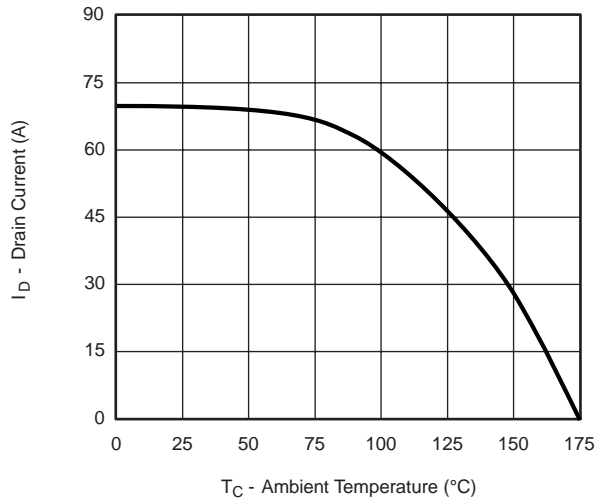


Avalanche Current vs. Time

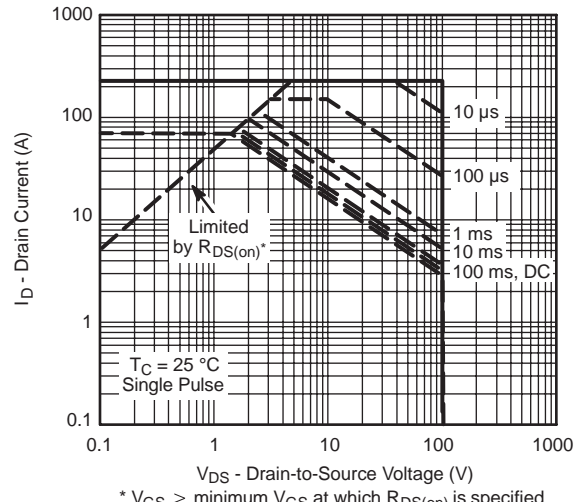


Drain Source Breakdown vs. Junction Temperature

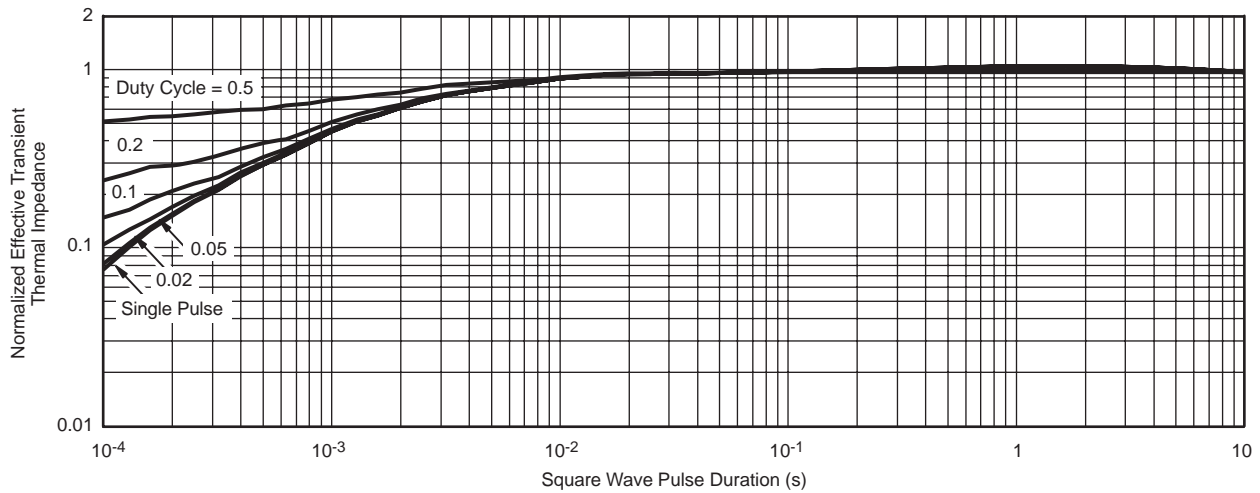
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature

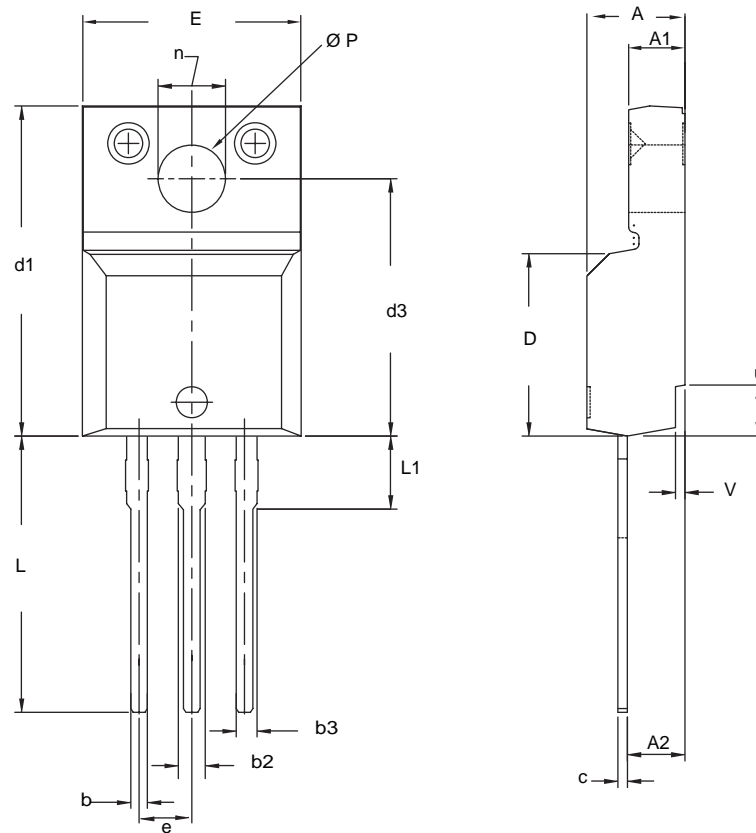


Safe Operating Area
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Case

TO-220 FULLPAK (HIGH VOLTAGE)



DIM.	MILLIMETERS	
	MIN.	MAX.
A	4.270	4.830
A1	2.450	2.830
A2	2.510	2.850
b	0.622	0.890
b2	1.229	1.450
b3	1.229	1.400
c	0.440	0.629
D	8.650	9.800
d1	15.68	16.220
d3	12.300	12.920
E	9.360	10.630
e	2.54 BSC	
L	12.200	13.730
L1	3.100	3.500
n	6.050	6.150
Ø P	3.050	3.450
u	2.400	2.500
v	0.400	0.500

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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