

## Dual N-Channel 30-V (D-S) MOSFET



**RoHS**  
COMPLIANT

PRODUCT SUMMARY			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
30	0.009 at $V_{GS} = 10$ V	45	8.1 nC
	0.012 at $V_{GS} = 4.5$ V	32	

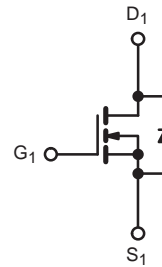
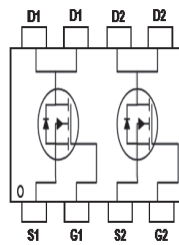
### FEATURES

- DT-Trench Power MOSFET
- 100 % UIS Tested
- 100 %  $R_g$  Tested

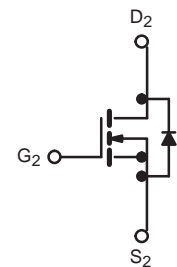
### APPLICATIONS

- Synchronous buck
- DC/DC conversion
- Half bridge
- POL

PDFN 3.3x3.3



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	30	V
Gate-source voltage	$V_{GS}$	+20	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	180	
Continuous source current (MOSFET diode conduction)	$I_S$	$T_C = 25$ °C	45
		$T_A = 25$ °C	3.9 <sup>b, c</sup>
Single pulse avalanche current	$I_{AS}$	10	
Single pulse avalanche energy	$E_{AS}$	19	mJ
Maximum power dissipation	$P_D$	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature)		260	

#### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s

THERMAL RESISTANCE RATINGS		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	27	34	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	6	7.5	

**Notes**

- a. Surface mounted on 1" x 1" FR4 board
- b. Maximum under steady state conditions is 69 °C/W

SPECIFICATIONS ( $T_J = 25$ °C, unless otherwise noted)						
PARAMETER	CHANNEL-1 AND CHANNEL-2					
	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	30	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	1	-	2.4	
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = +20$ V / -16 V	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 24$ V, $V_{GS} = 0$ V	-	-	1	$\mu$ A
		$V_{DS} = 24$ V, $V_{GS} = 0$ V, $T_J = 55$ °C	-	-	5	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	45	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 10$ A	-	0.0090	0.012	$\Omega$
		$V_{GS} = 4.5$ V, $I_D = 7$ A	-	0.0120	0.018	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10$ V, $I_D = 10$ A	-	57	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz	-	880	-	pF
Output capacitance	$C_{oss}$		-	250	-	
Reverse transfer capacitance	$C_{rss}$		-	30	-	
$C_{rss}/C_{iss}$ ratio			-	0.052	0.103	
Total gate charge	$Q_g$	$V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 10$ A	-	8.1	12.2	nC
Gate-source charge	$Q_{gs}$	$V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_D = 7$ A	-	3.7	4.5	
Gate-drain charge	$Q_{gd}$		-	0.67	-	
Gate resistance	$R_g$	$f = 1$ MHz	0.24	1.2	2.4	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15$ V, $R_L = 1.2$ $\Omega$ , $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$	-	10	20	ns
Rise time	$t_r$		-	6	12	
Turn-off delay time	$t_{d(off)}$		-	18	36	
Fall time	$t_f$		-	8	16	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15$ V, $R_L = 1.2$ $\Omega$ , $I_D \cong 7$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ $\Omega$	-	15	30	
Rise time	$t_r$		-	180	360	
Turn-off delay time	$t_{d(off)}$		-	20	40	
Fall time	$t_f$		-	15	30	

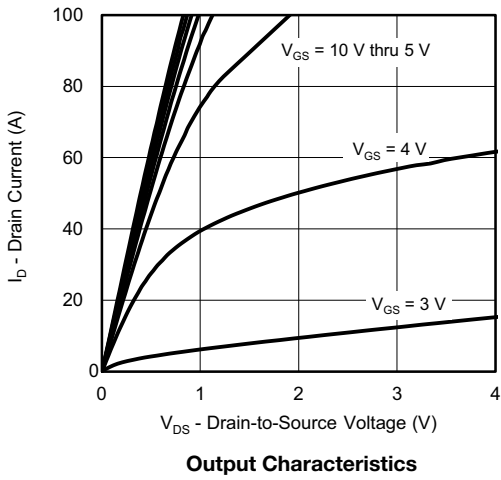
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Drain-source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	45	A
Pulse diode forward current	$I_{SM}$		-	-	180	
Body diode voltage	$V_{SD}$	$I_S = 12.5\text{ A}, V_{GS} = 0\text{ V}$	-	0.7	1.2	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 12.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	15	30	ns
Body diode reverse recovery charge	$Q_{rr}$		-	4.3	8.6	nC
Reverse recovery fall time	$t_a$		-	8	-	ns
Reverse recovery rise time	$t_b$		-	7	-	

**Notes**

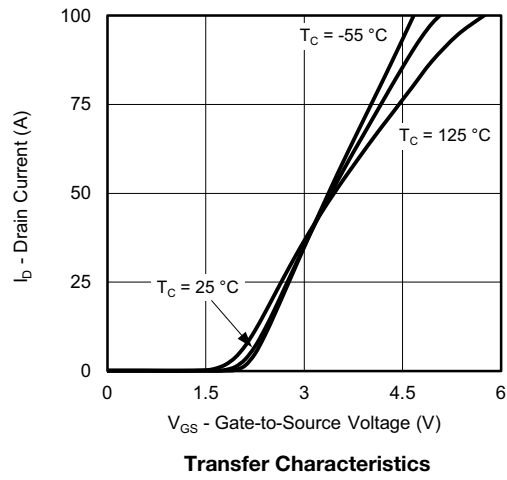
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- Guaranteed by design, not subject to production testing

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

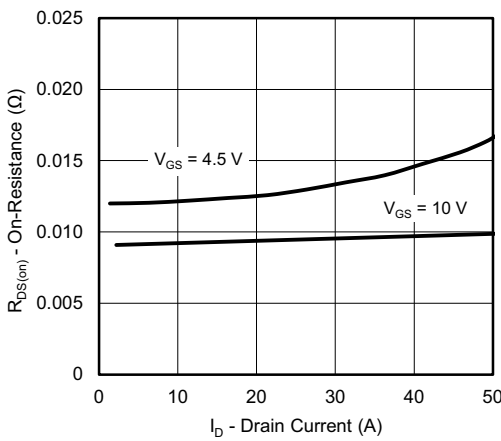
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



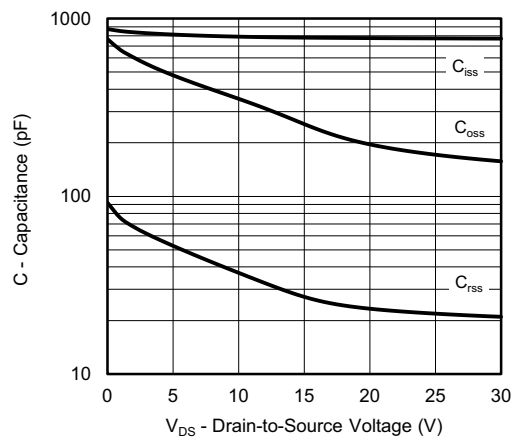
**Output Characteristics**



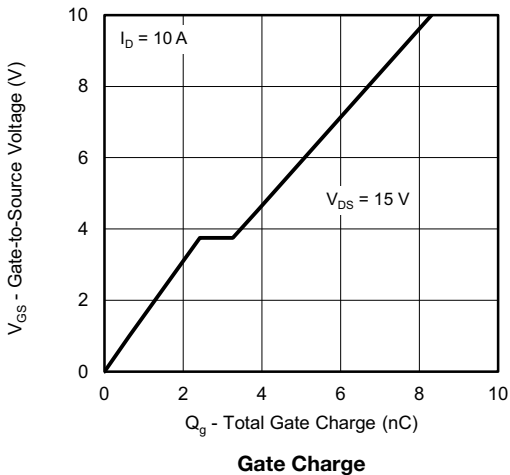
**Transfer Characteristics**



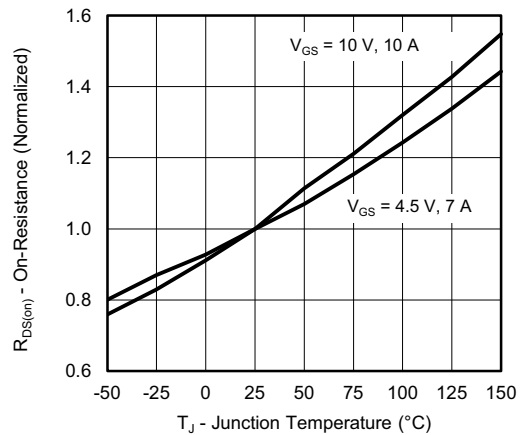
**On-Resistance vs. Drain Current and Gate**



**Capacitance**

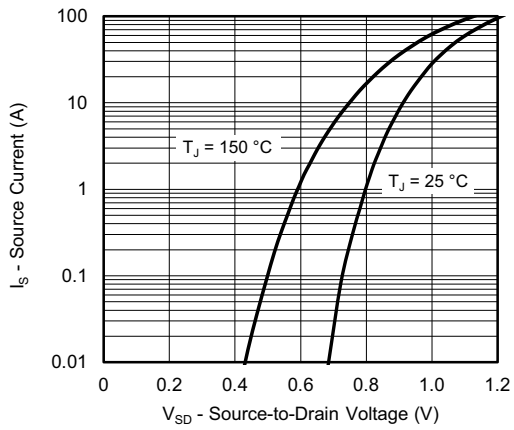


**Gate Charge**

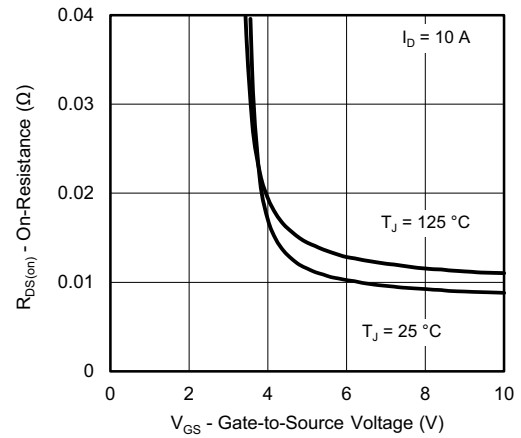


**On-Resistance vs. Junction Temperature**

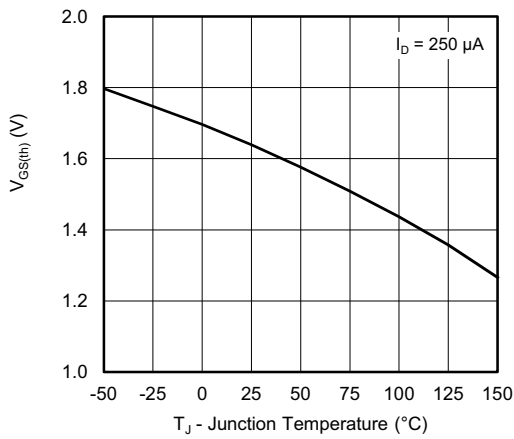
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



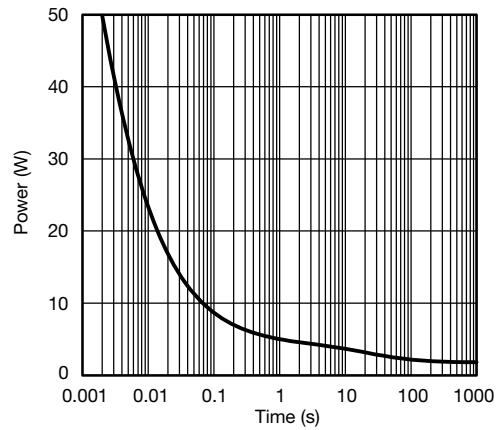
**Source-Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**

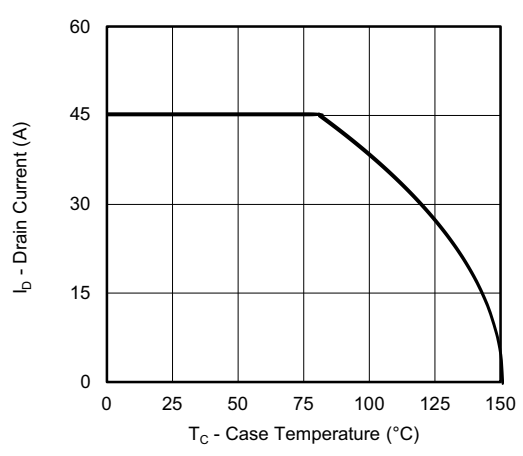


**Threshold Voltage**

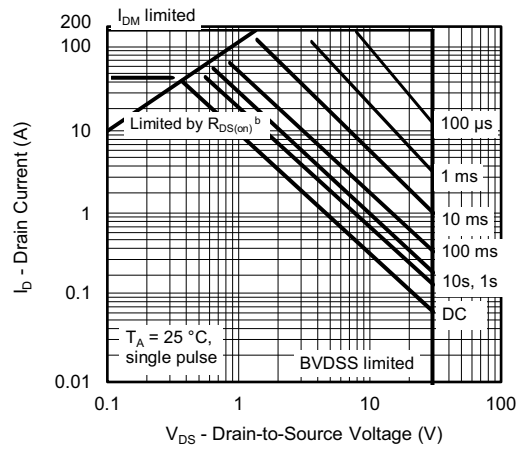


**Single Pulse Power**

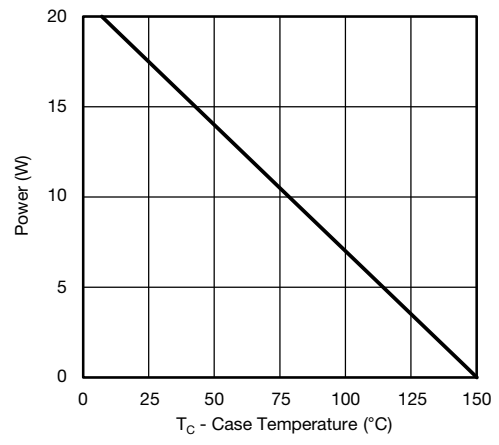
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



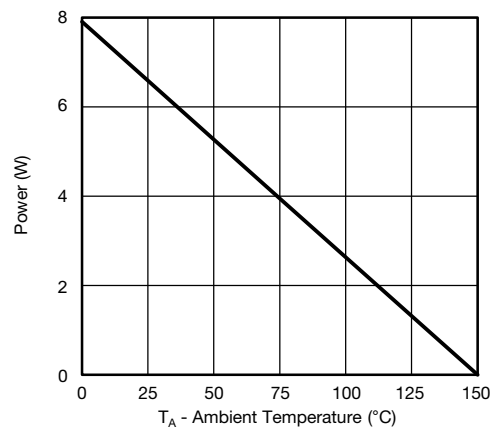
**Current Derating <sup>a</sup>**



**Safe Operating Area, Junction-to-Ambient**



**Power, Junction-to-Case**



**Power, Junction-to-Ambient**

**Notes**

- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit
- b.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

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