

## N-Channel 60 V (D-S) Super Junction Power MOSFET

### PRODUCT SUMMARY

V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (mΩ)(Typ.)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
60	1.5 at V <sub>GS</sub> = 10 V	220	205 nC
	2 at V <sub>GS</sub> = 4.5 V		

### FEATURES

- DT-SJ Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested
- Low RDS(ON)
- RoHS and Halogen-Free Compliant



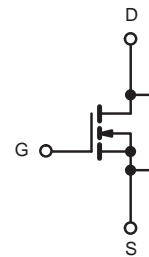
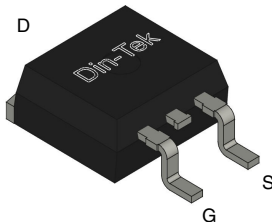
**RoHS**  
COMPLIANT

### APPLICATIONS

- High Frequency Switching and Synchronous Rectification
- BLDC

### TO-263 Pin Configuration

Top View



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 175 °C) <sup>a</sup>	I <sub>D</sub>	T <sub>C</sub> = 25 °C	A
		T <sub>C</sub> = 100 °C	
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	800	
Single Avalanche Energy	E <sub>AS</sub>	1900	mJ
Maximum Power Dissipation <sup>c</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	W
		T <sub>C</sub> = 100 °C	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient (PCB Mount) <sup>d</sup>	R <sub>thJA</sub>	50	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.57	

### Notes

- Calculated continuous current based on maximum allowable junction temperature.
- Repetitive rating; pulse width limited by max. junction temperature.
- P<sub>D</sub> is based on max. junction temperature, using junction-case thermal resistance.
- The value of R<sub>thJA</sub> is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>a</sub>=25 °C.

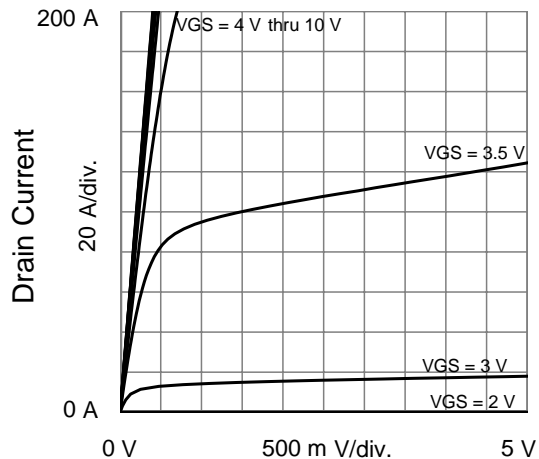
SPECIFICATIONS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	-	3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	220	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	1.5	2.2	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	-	2	3	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 5\text{ V}, I_D = 20\text{ A}$	-	50	-	S
<b>Dynamic <sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}, f = 1\text{ MHz}$	-	11500	-	pF
Output Capacitance	$C_{oss}$		-	2480	-	
Reverse Transfer Capacitance	$C_{rss}$		-	205	-	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	-	205	-	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$		-	25	-	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$		-	43	-	
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	-	0.8	-	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 20\text{ A}, R_g = 2.5\text{ }\Omega$ $V_{GS} = 10\text{ V}, R_L = 1.5\text{ }\Omega$	-	40	-	ns
Rise Time <sup>c</sup>	$t_r$		-	24	-	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$		-	108	-	
Fall Time <sup>c</sup>	$t_f$		-	30	-	
<b>Drain-Source Body Diode Ratings and Characteristics <sup>b</sup> (<math>T_C = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	220	A
Pulsed Current	$I_{SM}$		-	-	800	A
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 1\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	33	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	80	-	nC

**Notes**

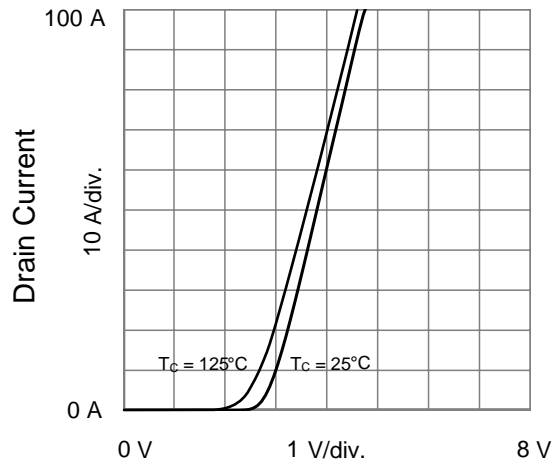
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.  
 c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

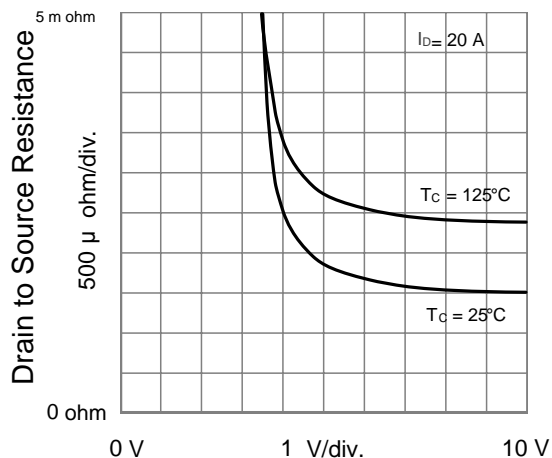
**TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**



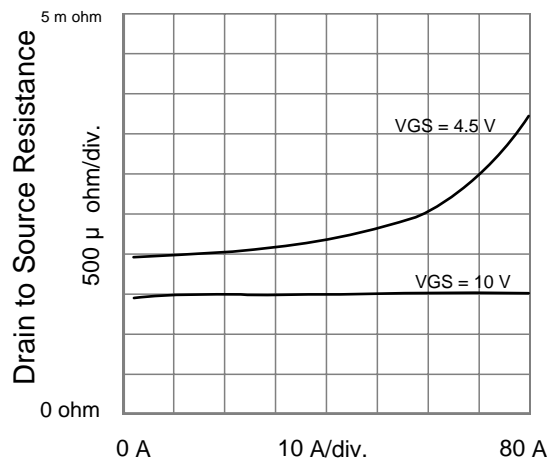
**Drain to Source Voltage  
Output Characteristics**



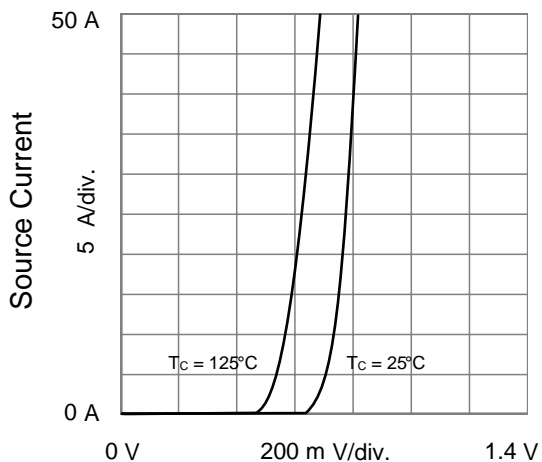
**Gate to Source Voltage  
Transfer Characteristics**



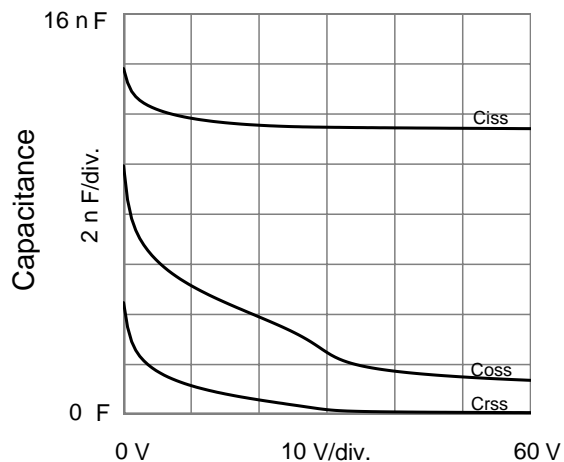
**Gate to Source Voltage  
Drain to Source Resistance vs. Gate to Source Voltage**



**Drain Current**

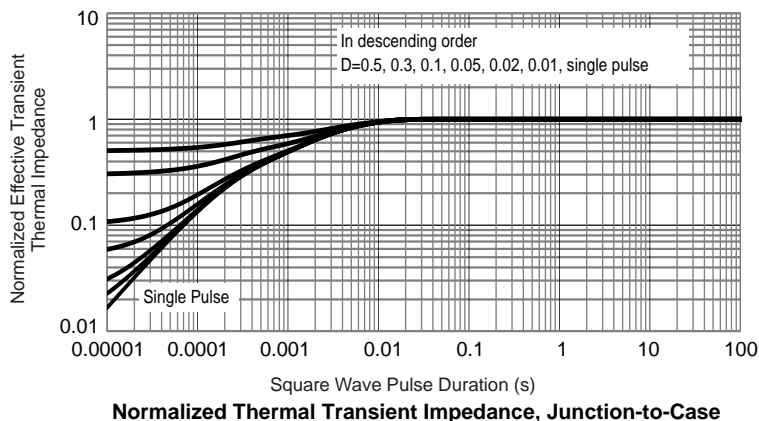
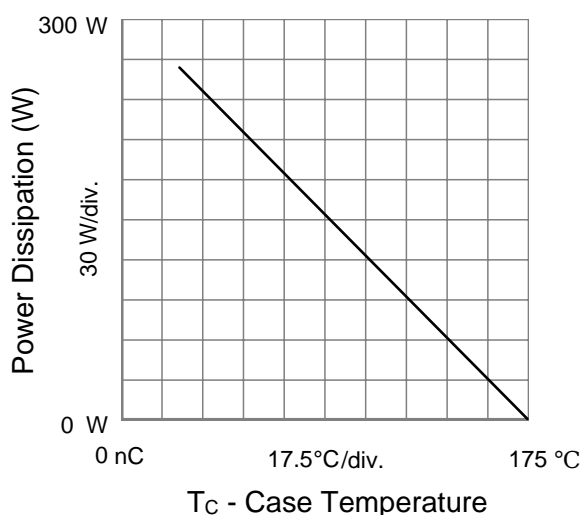
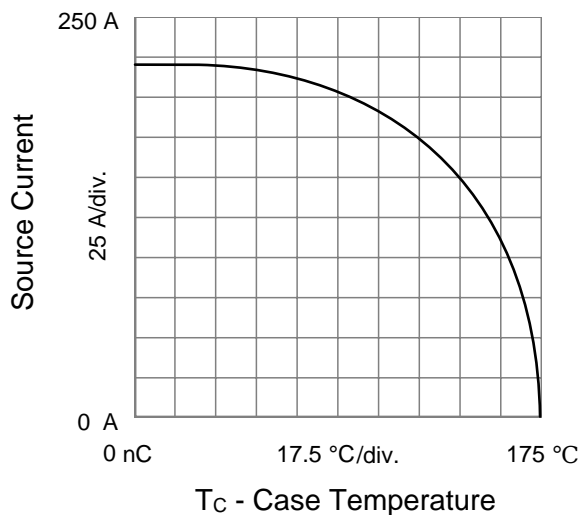
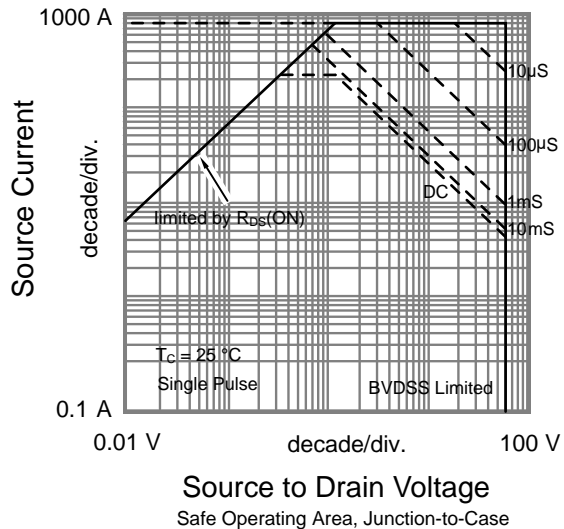
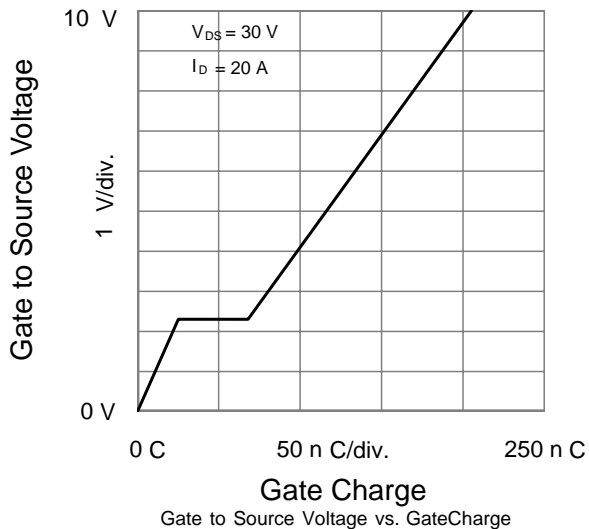


**Source to Drain Voltage  
Body Diode Forward Characteristics**

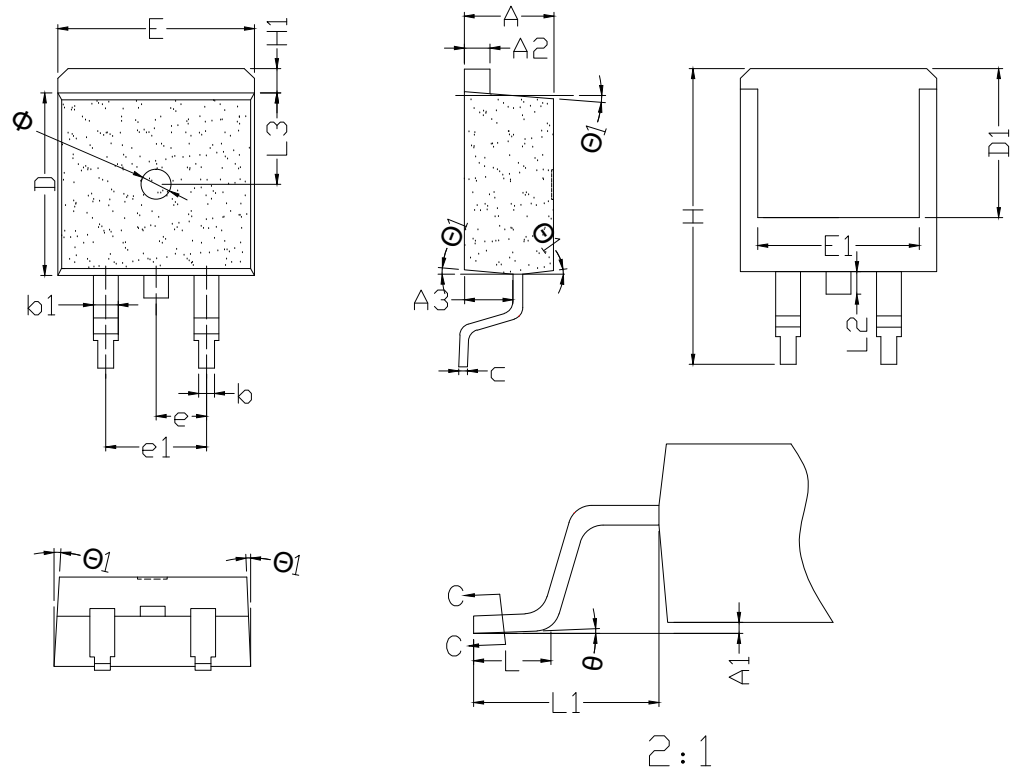


**Drain to Source Voltage  
Capacitances**

**TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**



## TO-263 PACKAGE OUTLINE



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX	SYMBOL	MIN	TYP	MAX
A	4.10	4.50	4.80	e	2.35	2.54	2.75
A1	0.00	0.10	0.30	e1	5.08REF		
A2	1.10	1.30	1.50	H	14.50	15.15	16.00
A3	2.15	2.50	3.10	H1	1.00	1.28	1.75
b	0.60	0.80	1.05	L	1.80	2.23	2.90
b1	1.05	1.33	1.50	L1	4.30	4.75	5.50
c	0.33	0.50	0.66	L2	1.00	1.30	1.85
D	8.40	9.20	9.60	L3	0.90	4.65	9.00
D1	7.50REF			phi	0°	2°	5°
E	9.60	10.02	10.80	phi1	2°	-	7°
E1	7.60	9.88	10.30	Phi	1.5BSC		

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