

**N-Channel 600V (D-S) Super Junction Power MOSFET**

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	600	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	2.3
Q <sub>g</sub> (Max.) (nC)	31	
Q <sub>gs</sub> (nC)	4.6	
Q <sub>gd</sub> (nC)	17	
Configuration	Single	

**FEATURES**

- Isolated Package
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available

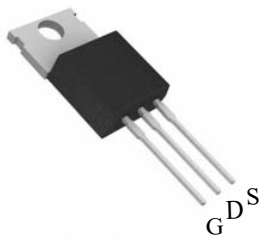


**RoHS\***  
COMPLIANT

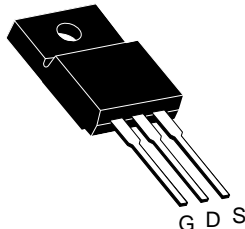
TO-220 Pin Configuration

TO-220 FULLPAK

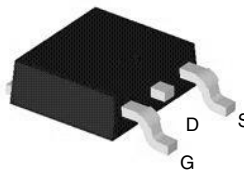
TO-252 Pin Configuration TO-251



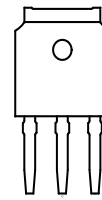
Top View



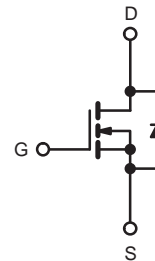
Top View



Top View



G D S



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>C</sub> = 25 °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V <sub>DS</sub>	600	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	2.0	A
		T <sub>C</sub> = 100 °C	1.6	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	10		
Linear Derating Factor		0.28	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	250	mJ	
Repetitive Avalanche Current <sup>a</sup>	I <sub>AR</sub>	2.5	A	
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	3.5	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	35	W
Peak Diode Recovery dV/dt <sup>c</sup>		dV/dt	3.0	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>		- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw		10	
			1.1	N · m

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 73 mH, R<sub>G</sub> = 25 Ω, I<sub>AS</sub> = 1.5 A (see fig. 12).
- I<sub>SD</sub> ≤ 1.6 A, dI/dt ≤ 60 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.6	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.62	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	100	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.5\text{ A}^b$	-	2.3	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 1.5\text{ A}^b$		2.2	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	660	-	pF
Output Capacitance	$C_{oss}$			-	86	-	
Reverse Transfer Capacitance	$C_{rss}$			-	19	-	
Drain to Sink Capacitance	$C$	$f = 1.0\text{ MHz}$		-	12	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 1.6\text{ A}, V_{DS} = 360\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	31	nC
Gate-Source Charge	$Q_{GS}$			-	-	4.6	
Gate-Drain Charge	$Q_{GD}$			-	-	17	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 1.6\text{ A}, R_G = 12\text{ }\Omega, R_D = 82\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	11	-	ns
Rise Time	$t_r$			-	13	-	
Turn-Off Delay Time	$t_{d(off)}$			-	35	-	
Fall Time	$t_f$			-	14	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.0	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	10	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 1.5\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 1.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	400	810	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	2.1	4.2	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

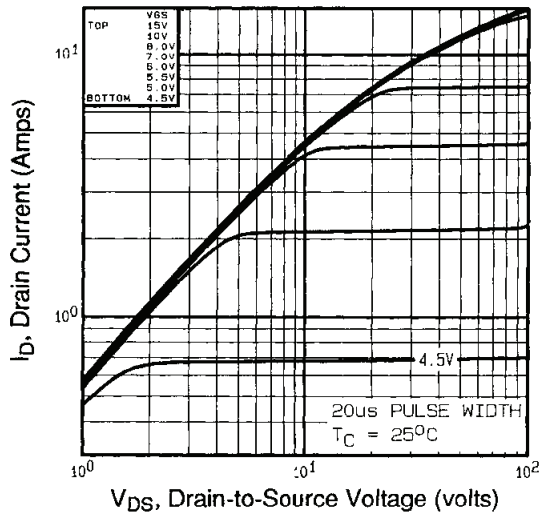


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

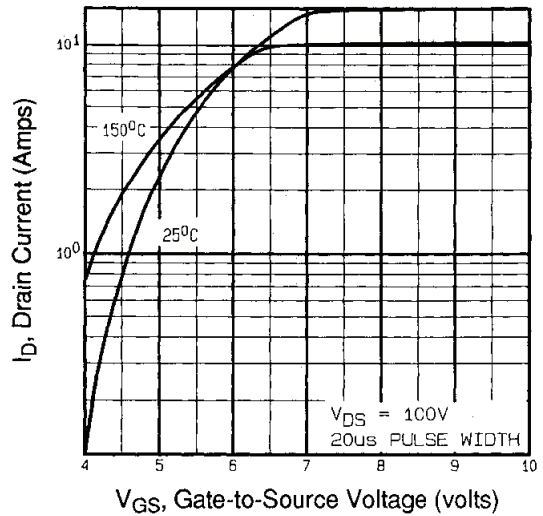


Fig. 3 - Typical Transfer Characteristics

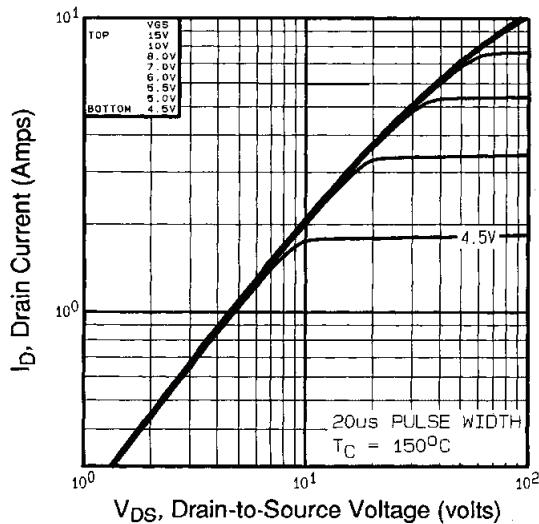


Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$

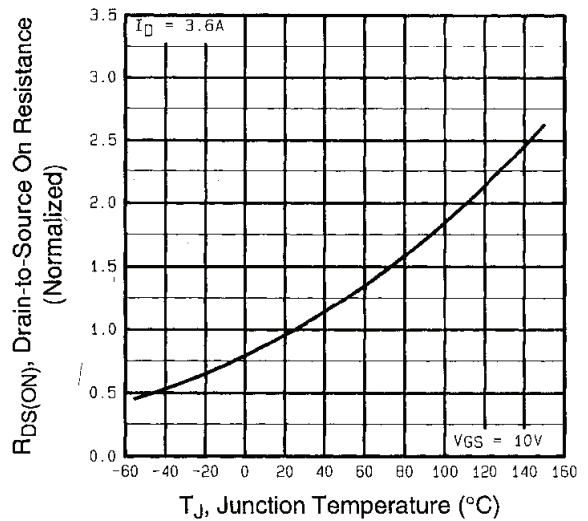


Fig. 4 - Normalized On-Resistance vs. Temperature

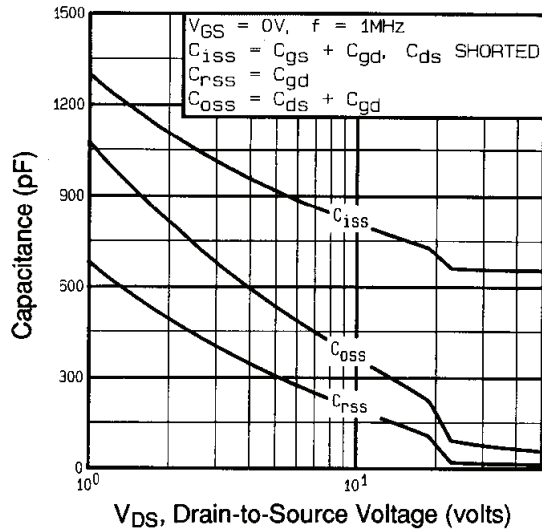


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

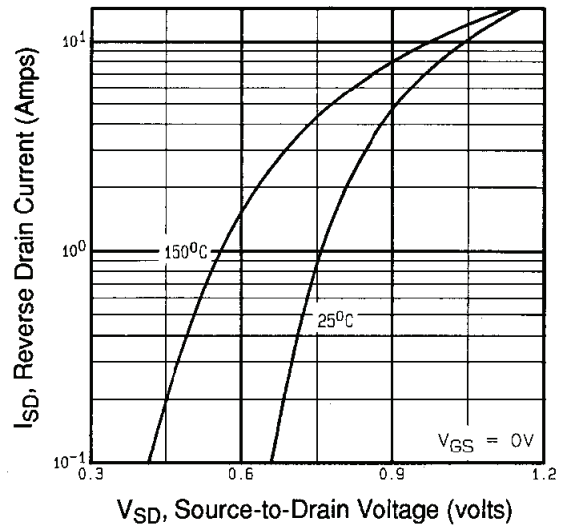


Fig. 7 - Typical Source-Drain Diode Forward Voltage

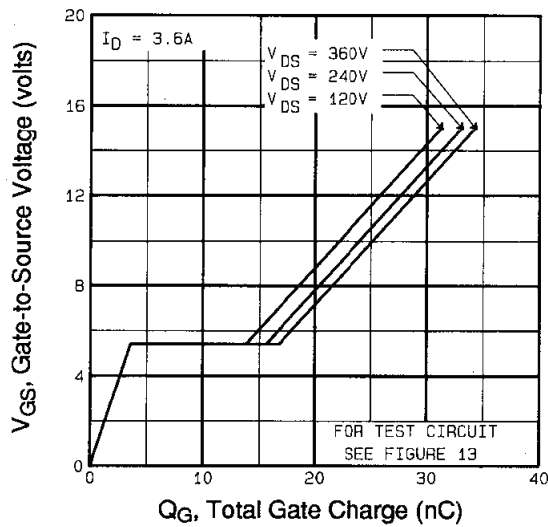


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

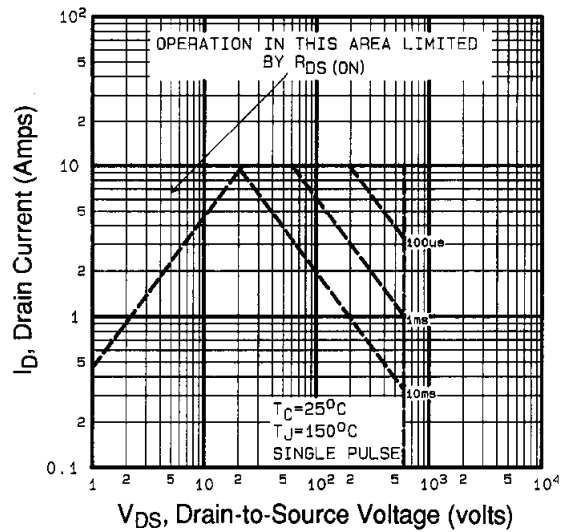


Fig. 8 - Maximum Safe Operating Area

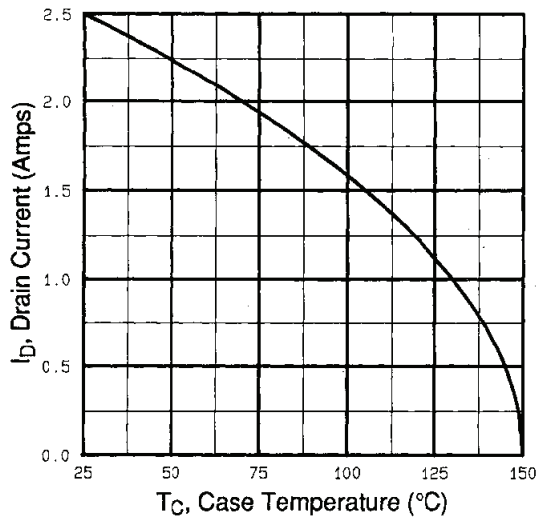


Fig. 9 - Maximum Drain Current vs. Case Temperature

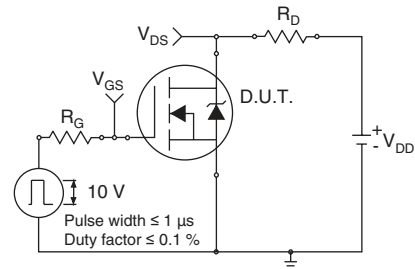


Fig. 10a - Switching Time Test Circuit

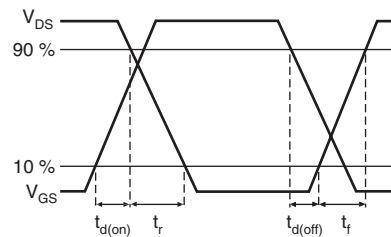


Fig. 10b - Switching Time Waveforms

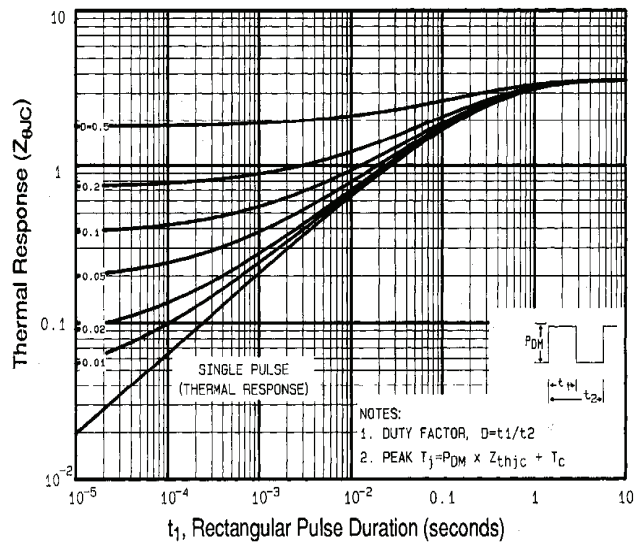


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

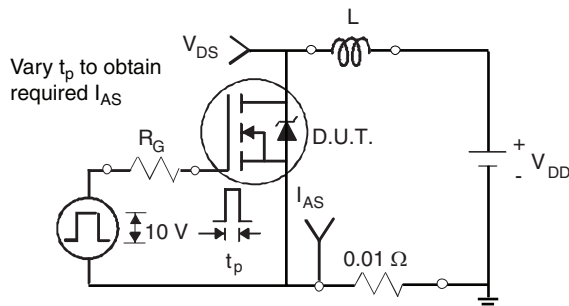


Fig. 12a - Unclamped Inductive Test Circuit

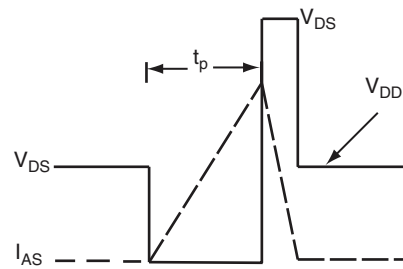


Fig. 12b - Unclamped Inductive Waveforms

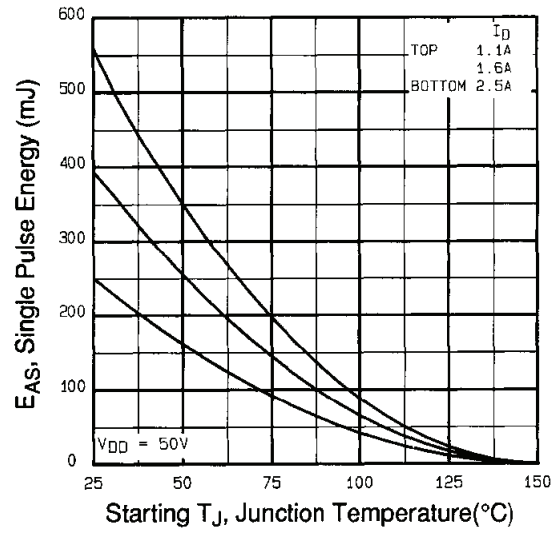


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

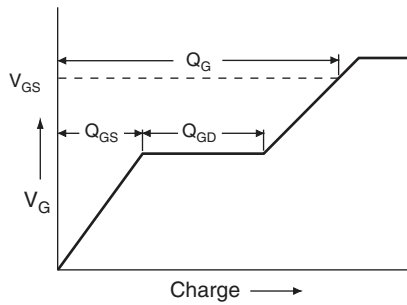


Fig. 13a - Basic Gate Charge Waveform

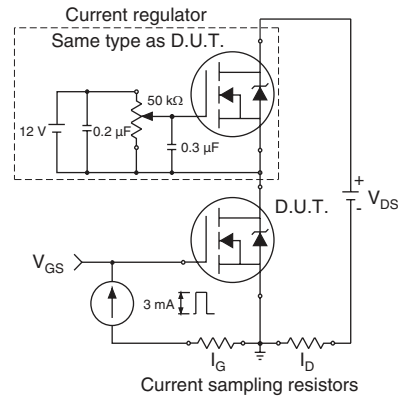
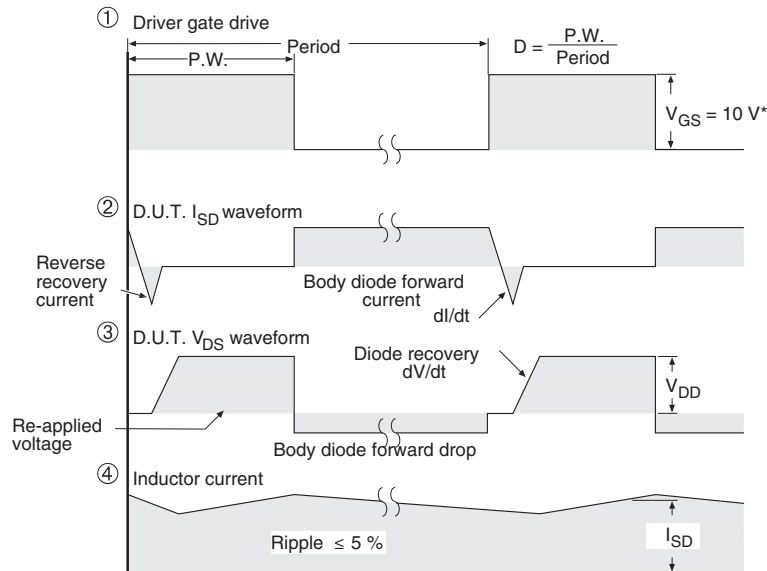
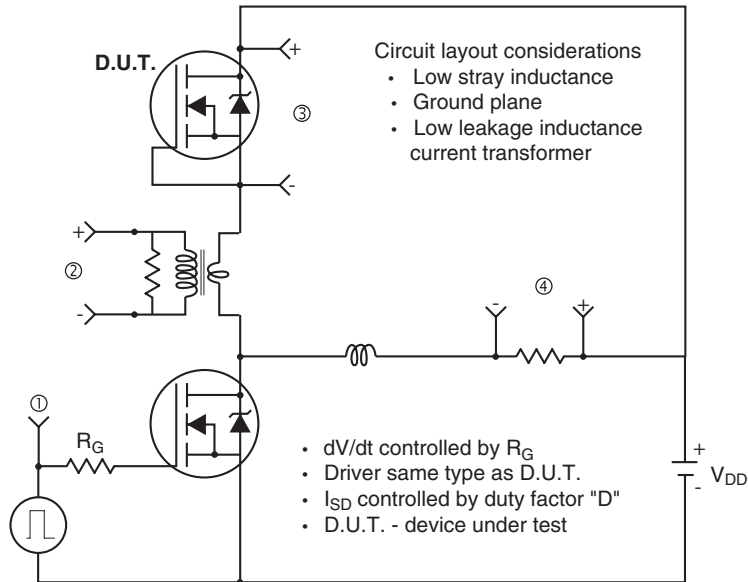


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**



\*  $V_{GS} = 5\text{ V}$  for logic level devices and  $3\text{ V}$  drive devices

**Fig. 14 - For N-Channel**

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