

**Power MOSFET**

PRODUCT SUMMARY	
$V_{DS}$ (V)	600
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 2.2
$Q_g$ (Max.) (nC)	39
$Q_{gs}$ (nC)	10
$Q_{gd}$ (nC)	19
Configuration	Single

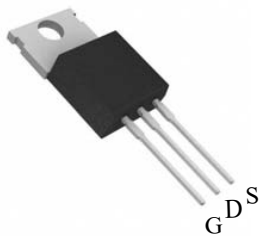
**FEATURES**

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V,  $V_{GS}$  Rating
- Reduced  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



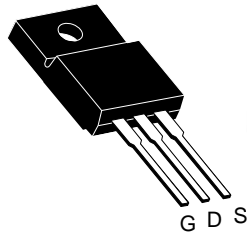
Available  
**RoHS\***  
COMPLIANT

TO-220 Pin Configuration



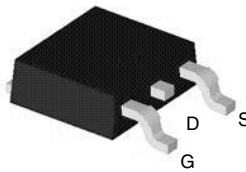
Top View

TO-220 FULLPAK



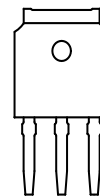
Top View

TO-252 Pin Configuration

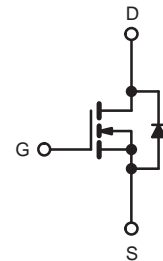


Top View

TO-251



G D S



N-Channel MOSFET

**DTP4N60 DTP4N60F DTU4N60 DTL4N60**

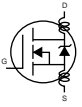
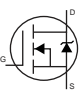
ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	600	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	4	
		$T_C = 100\text{ }^\circ\text{C}$	2.9	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	25	A	
Linear Derating Factor		1.0	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	530	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	6.2	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	13	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	125	W
Peak Diode Recovery $dV/dt^c$		$dV/dt$	3.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 25\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 6.2\text{ A}$  (see fig. 12).
- $I_{SD} \leq 6.2\text{ A}$ ,  $dI/dt \leq 80\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

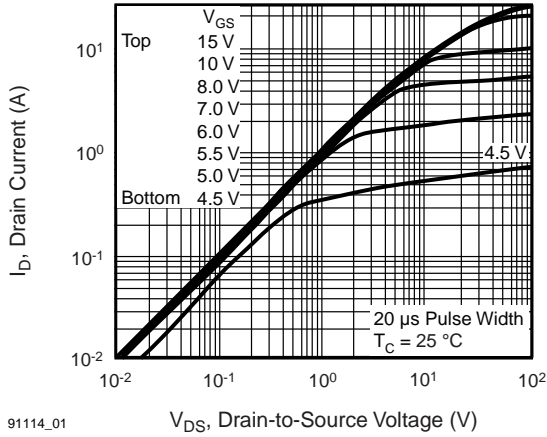
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.70	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	100	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3.7\text{ A}^b$	-	-	2.2	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 100\text{ V}, I_D = 3.7\text{ A}^b$	3.7	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$	-	1100	-	pF
Output Capacitance	$C_{oss}$		-	140	-	
Reverse Transfer Capacitance	$C_{rss}$		-	15	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 4\text{ A}, V_{DS} = 360\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	39	nC
Gate-Source Charge	$Q_{gs}$		-	-	10	
Gate-Drain Charge	$Q_{gd}$		-	-	19	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 4\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 47\text{ }\Omega, \text{ see fig. 10}^b$	-	12	-	ns
Rise Time	$t_r$		-	20	-	
Turn-Off Delay Time	$t_{d(off)}$		-	27	-	
Fall Time	$t_f$		-	17	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	$L_S$		-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	4.0	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	25	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 4\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 4\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	440	680	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	2.1	3.2	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

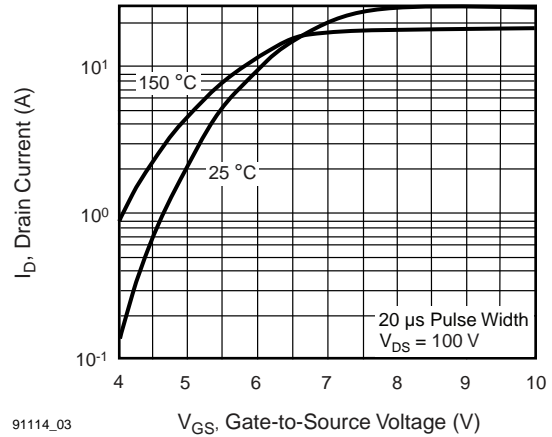
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



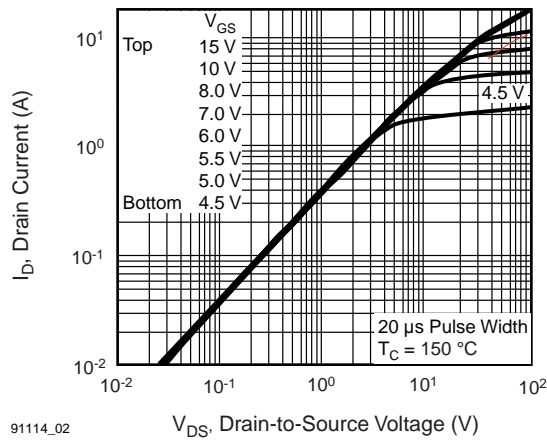
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**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



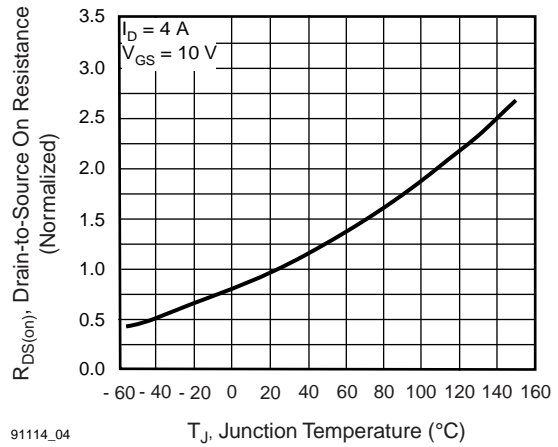
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**Fig. 3 - Typical Transfer Characteristics**



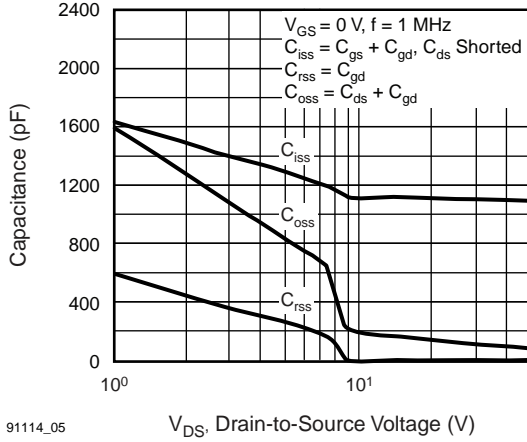
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**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**



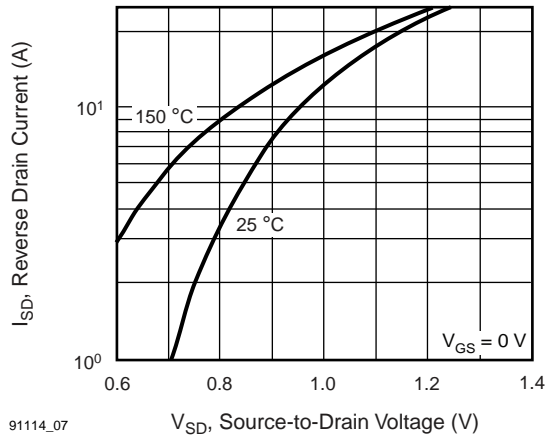
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**Fig. 4 - Normalized On-Resistance vs. Temperature**



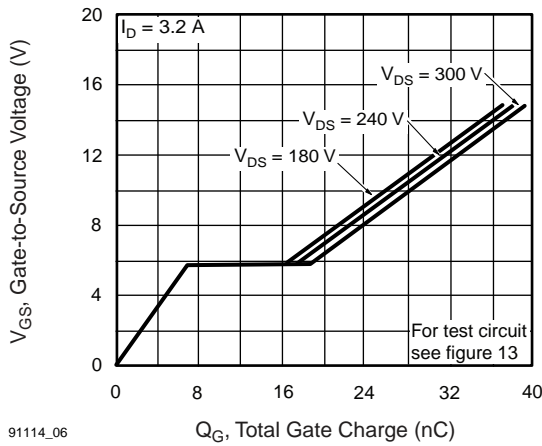
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**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



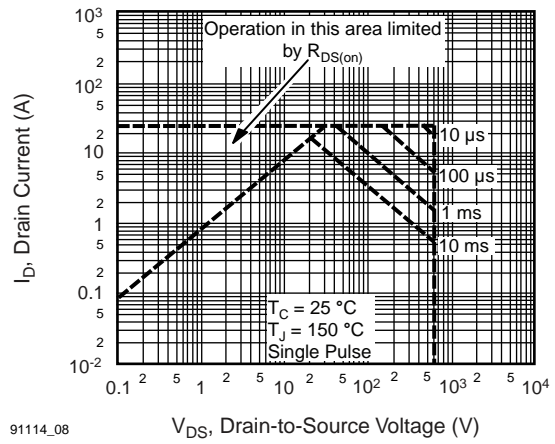
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**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



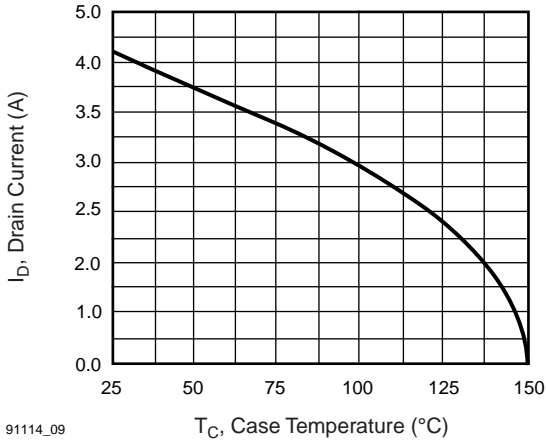
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**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



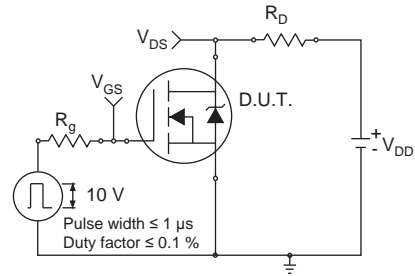
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**Fig. 8 - Maximum Safe Operating Area**

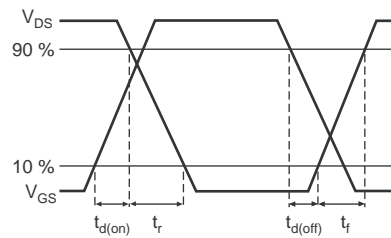


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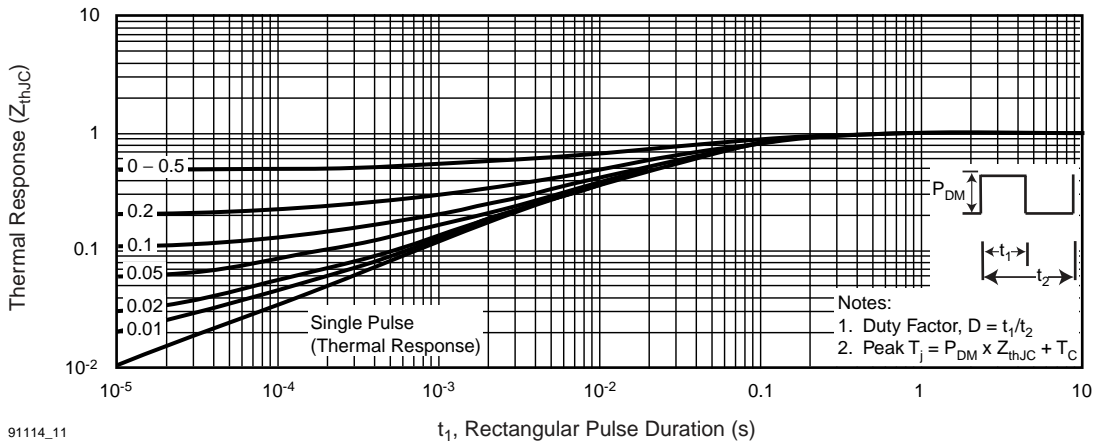
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**

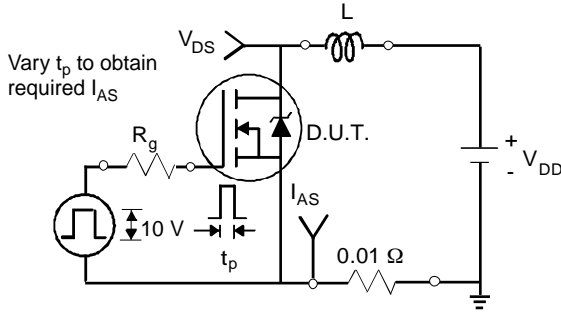


**Fig. 10b - Switching Time Waveforms**

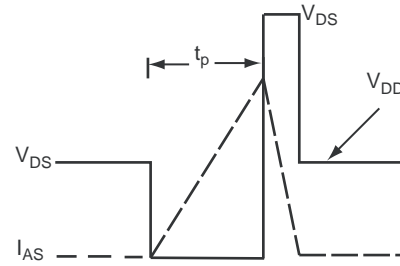


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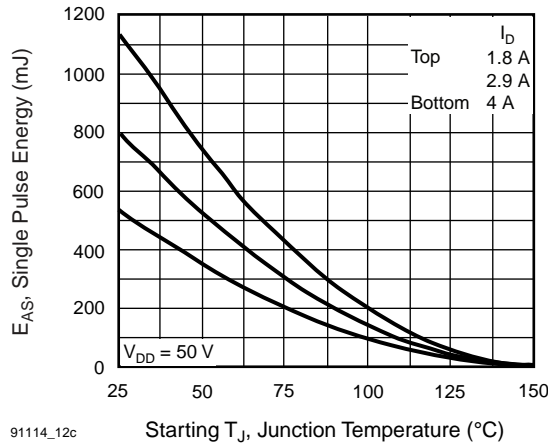
**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



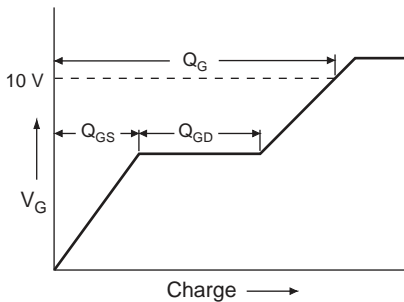
**Fig. 12a - Unclamped Inductive Test Circuit**



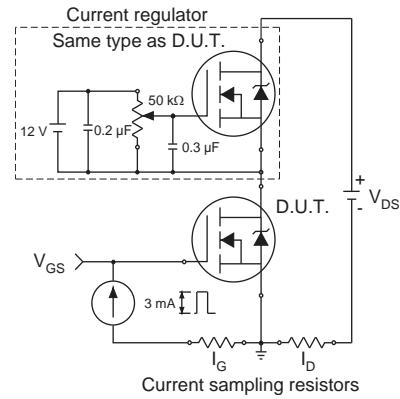
**Fig. 12b - Unclamped Inductive Waveforms**



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**



**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**

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