

## N-Channel 500V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V) at T <sub>J</sub> max.	500
R <sub>DS(on)</sub> max. at 25 °C (Ω)	V <sub>GS</sub> = 10 V   0.380
Q <sub>g</sub> max. (nC)	50
Q <sub>gs</sub> (nC)	6
Q <sub>gd</sub> (nC)	10
Configuration	Single

### FEATURES

- Low figure-of-merit (FOM) R<sub>on</sub> x Q<sub>g</sub>
- Low input capacitance (C<sub>iss</sub>)
- Reduced switching and conduction losses
- Low gate charge (Q<sub>g</sub>)
- Avalanche energy rated (UIS)

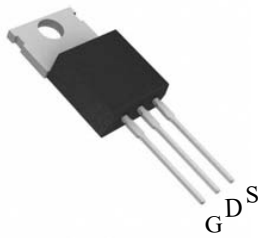


**RoHS**  
COMPLIANT

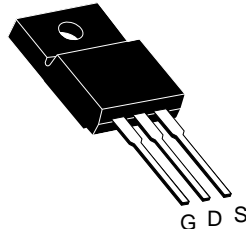
### APPLICATIONS

- Computing
  - PC silver box / ATX power supplies
- Lighting
  - Two stage LED lighting
- Consumer electronics

TO-220 Pin Configuration

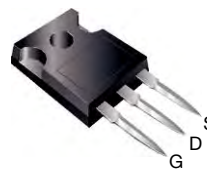


TO-220 FULLPAK

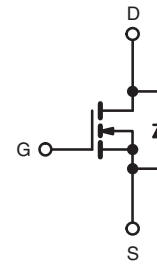


Top View

TO-247AC



Top View




N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	500	V
Gate-Source Voltage	V <sub>GS</sub>	± 30	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	11
		T <sub>C</sub> = 100 °C	6.6
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	21	A
Linear Derating Factor		0.91	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	103	mJ
Maximum Power Dissipation	P <sub>D</sub>	114	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	V <sub>DS</sub> = 0 V to 80 % V <sub>DS</sub>	70
Reverse Diode dV/dt <sup>d</sup>		27	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s	300	°C

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 28.2 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 2.7 A.
- 1.6 mm from case.
- I<sub>SD</sub> ≤ I<sub>D</sub>, dI/dt = 100 A/μs, starting T<sub>J</sub> = 25 °C.

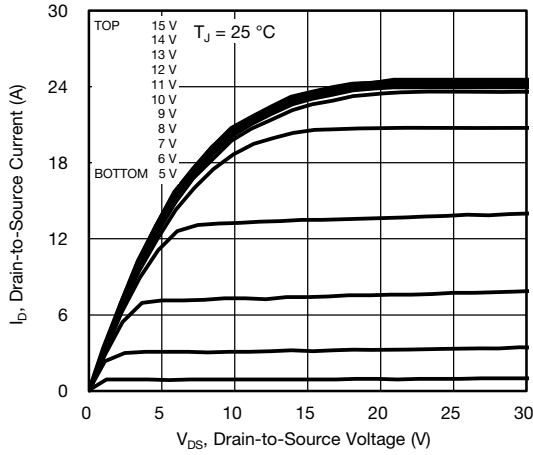
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	62	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	1.1	

<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.60	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$	-	0.380	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 30\text{ V}, I_D = 6\text{ A}$	-	3.1	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$	-	886	-	pF
Output Capacitance	$C_{oss}$		-	52	-	
Reverse Transfer Capacitance	$C_{rss}$		-	6	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$		$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	45	
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$		-	131	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}, V_{DS} = 400\text{ V}$	-	25	50	nC
Gate-Source Charge	$Q_{gs}$		-	6	-	
Gate-Drain Charge	$Q_{gd}$		-	10	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$	-	13	26	ns
Rise Time	$t_r$		-	16	32	
Turn-Off Delay Time	$t_{d(off)}$		-	29	58	
Fall Time	$t_f$		-	12	24	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$	-	0.92	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	11	A
Pulsed Diode Forward Current	$I_{SM}$		-	-	21	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 7.5\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 6\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$	-	244	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	2.5	-	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$		-	19	-	A

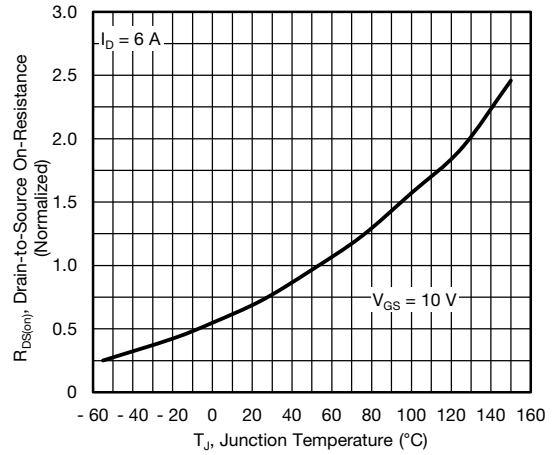
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

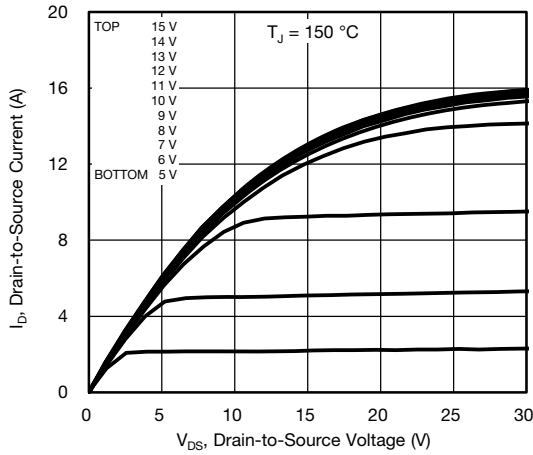
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



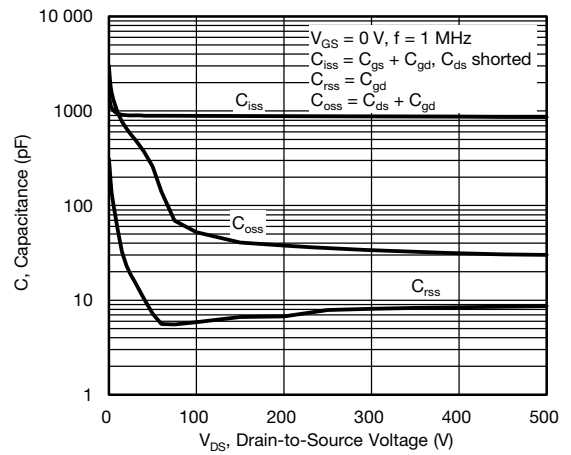
**Fig. 1 - Typical Output Characteristics**



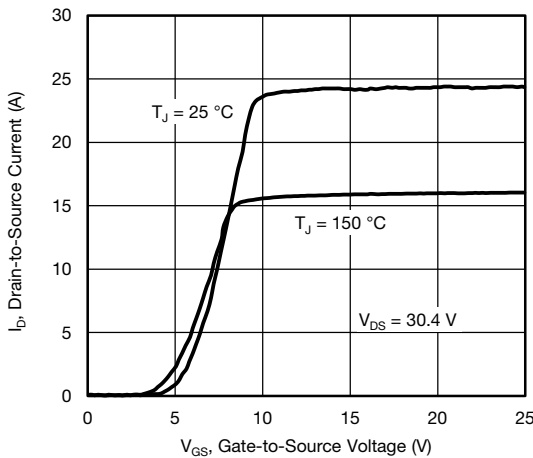
**Fig. 4 - Normalized On-Resistance vs. Temperature**



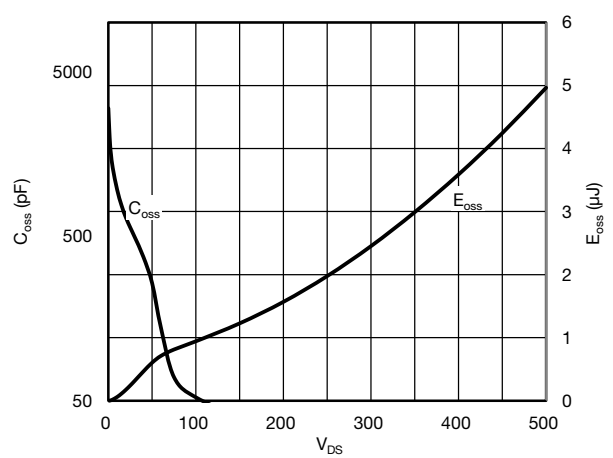
**Fig. 2 - Typical Output Characteristics**



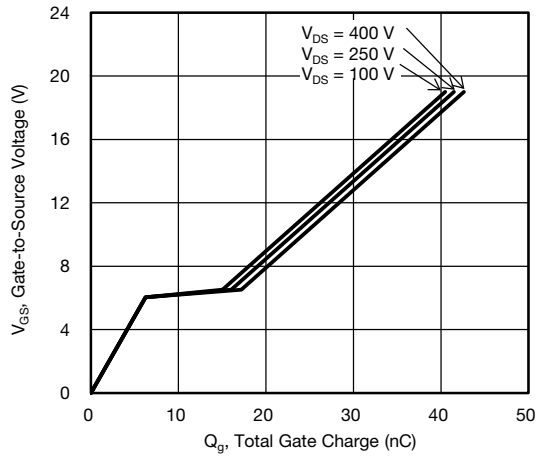
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



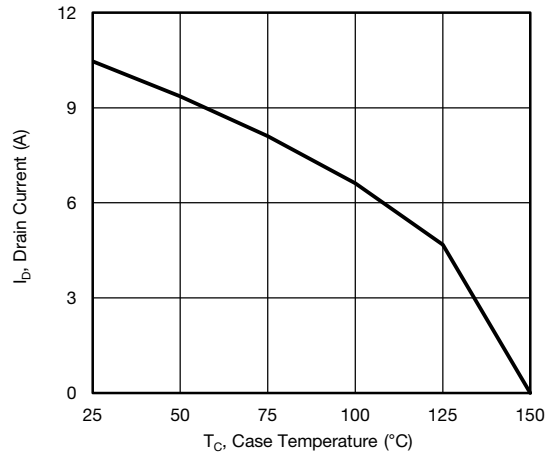
**Fig. 3 - Typical Transfer Characteristics**



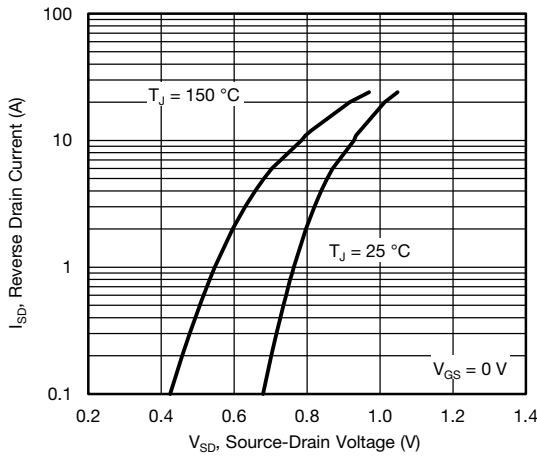
**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**



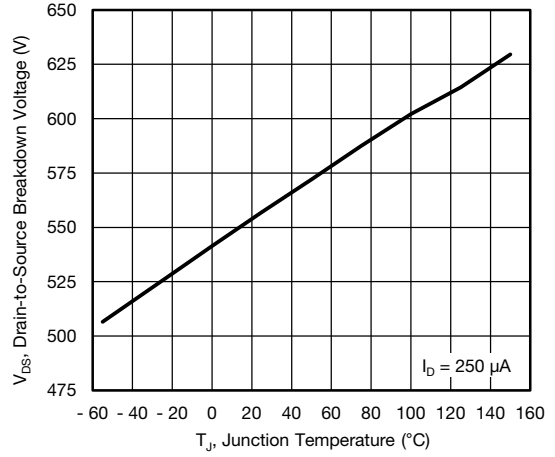
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



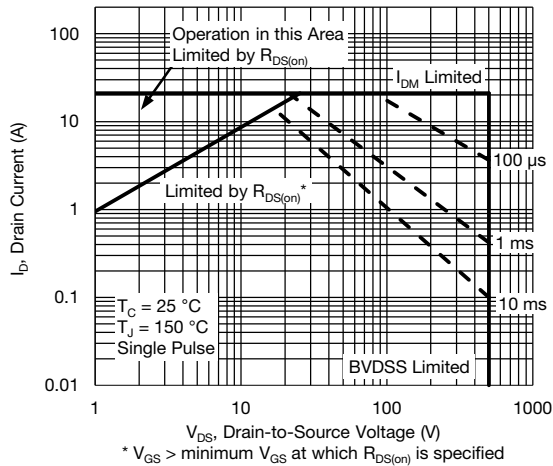
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



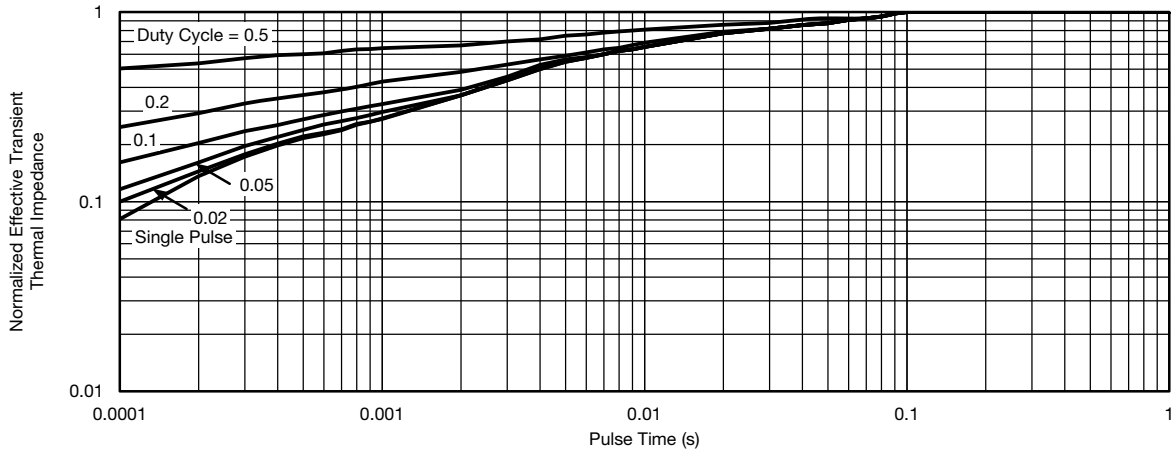
**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



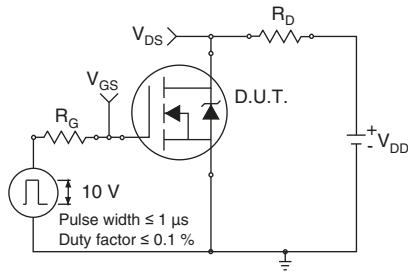
**Fig. 11 - Temperature vs. Drain-to-Source Voltage**



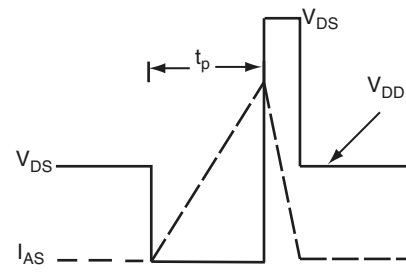
**Fig. 9 - Maximum Safe Operating Area**



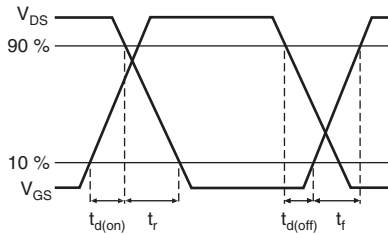
**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**



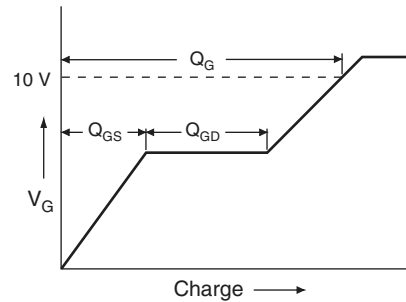
**Fig. 13 - Switching Time Test Circuit**



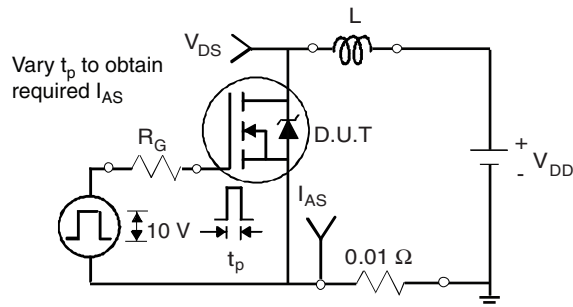
**Fig. 16 - Unclamped Inductive Waveforms**



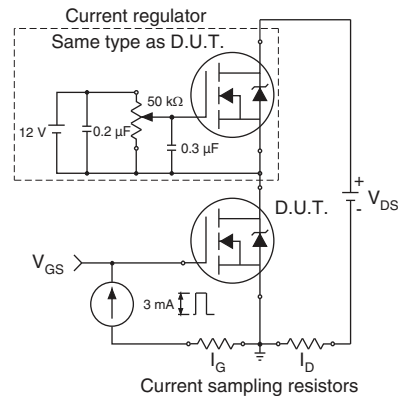
**Fig. 14 - Switching Time Waveforms**



**Fig. 17 - Basic Gate Charge Waveform**

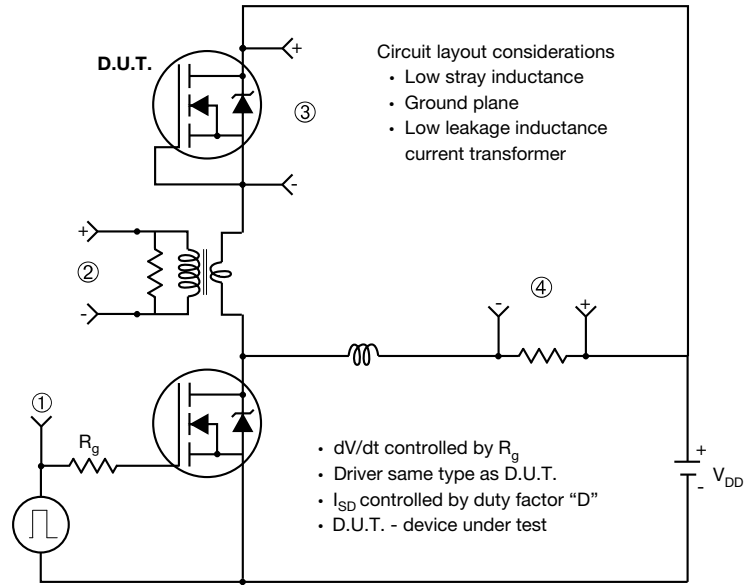


**Fig. 15 - Unclamped Inductive Test Circuit**



**Fig. 18 - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 19 - For N-Channel**

## Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Din-Tek Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Din-Tek"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Din-Tek makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Din-Tek disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Din-Tek's knowledge of typical requirements that are often placed on Din-Tek products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Din-Tek's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Din-Tek products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Din-Tek product could result in personal injury or death. Customers using or selling Din-Tek products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Din-Tek personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Din-Tek. Product names and markings noted herein may be trademarks of their respective owners.

## Material Category Policy

**Din-Tek Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.**

**Please note that some Din-Tek documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Din-Tek Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Din-Tek documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**