Din-Tek SEMICONDUCTOR

DTP5N65SJ/DTP5N65FSJ/DTU5N65SJ/DTL5N65SJ

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N-Channel 650V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	650	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.95
Q_g (Max.) (nC)	15	
Q_{gs} (nC)	3	
Q_{gd} (nC)	6	
Configuration	Single	

FEATURES

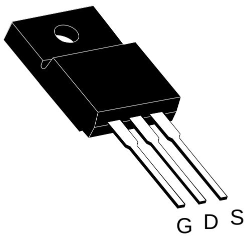
- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC

Available

RoHS* COMPLIANT

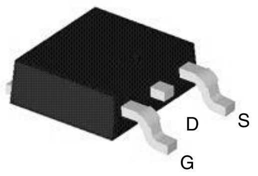
TO-220 Pin Configuration

TO-220 FULLPAK



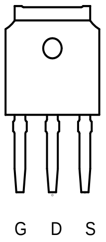
Top View

TO-252 Pin Configuration

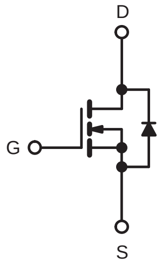


Top View

TO-251



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	650	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current[e]	V_{GS} at 10 V	T_C = 25 °C	I_D	5	A
Continuous Drain Current		T_C = 100 °C		4	
Pulsed Drain Current[a]			I_{DM}	16	
Linear Derating Factor				1.67/0.8/0.3	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	120	mJ
Repetitive Avalanche Current[a]			I_{AR}	34	A
Repetitive Avalanche Energy[a]			E_{AR}	17	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	205/35/30	W
Peak Diode Recovery dV/dt[c]			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)[d]	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

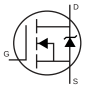
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 24 mH, R_G = 25 Ω, I_{AS} = 3.2 A (see fig. 12).
c. $I_{SD} \leq 3.2$ A, dI/dt $\leq$ 90 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
d. 1.6 mm from case.
e. Drain current limited by maximum junction temperature.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.6/1.2/0.6	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA[d]		-	0.6	-	mV/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V		-	-	10	µA
		V_{DS} = 520 V, V_{GS} = 0 V, T_J = 125 °C		-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 2.5 A[b]	-	0.95	-	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 2.5 A		8	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	320	-	pF
Output Capacitance	C_{oss}			-	75	-	
Reverse Transfer Capacitance	C_{rss}			-	4	-	
Output Capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = 1.0 V, f = 1.0 MHz	-	500	-	
			V_{DS} = 520 V, f = 1.0 MHz	-	83	-	
Effective Output Capacitance	C_{oss} eff.		V_{DS} = 0 V to 520 V[c]	-	14	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 2.5 A, V_{DS} = 400 V see fig. 6 and 13[b]	-	-	15	nC
Gate-Source Charge	Q_{gs}			-	-	3	
Gate-Drain Charge	Q_{gd}			-	-	6	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 325 V, I_D = 3.2 A R_G = 9.1 Ω, R_D = 62 Ω, see fig. 10[b]		-	18	-	ns
Rise Time	t_r			-	40	-	
Turn-Off Delay Time	$t_{d(off)}$			-	50	-	
Fall Time	t_f			-	30	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	16	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 3.2 A, V_{GS} = 0 V[b]		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 3.2 A, dI/dt = 100 A/µs[b]		-	180	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	2.1	3.2	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.
c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.
d. t = 60 s, f = 60 Hz.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

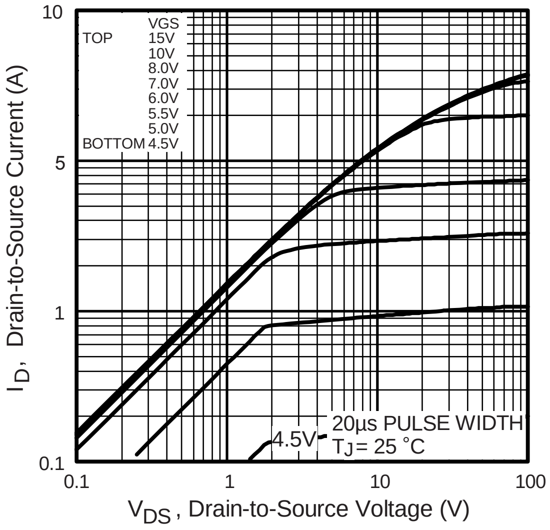


Fig. 1 - Typical Output Characteristics

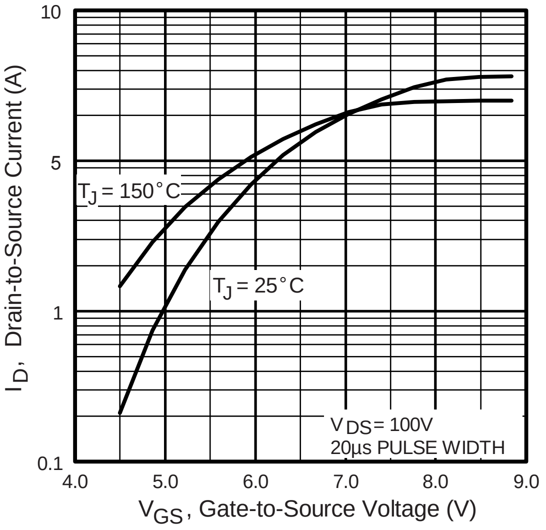


Fig. 3 - Typical Transfer Characteristics

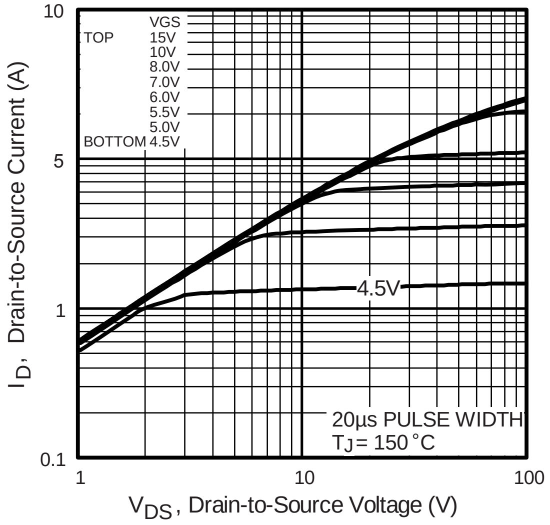


Fig. 2 - Typical Output Characteristics

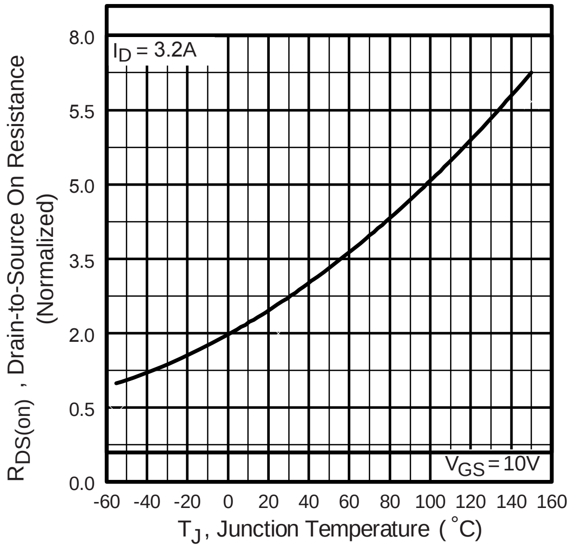


Fig. 4 - Normalized On-Resistance vs. Temperature

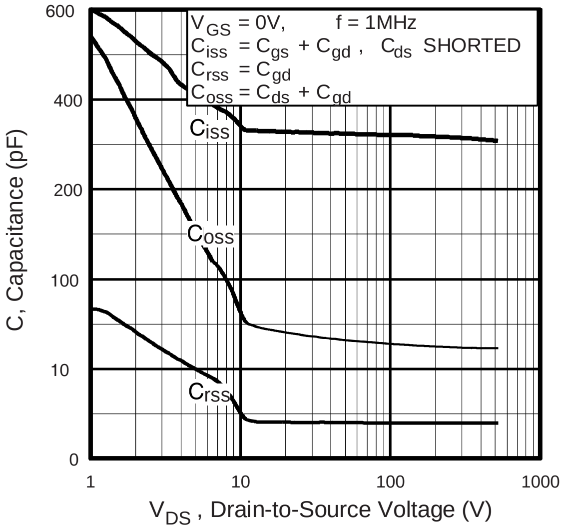


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

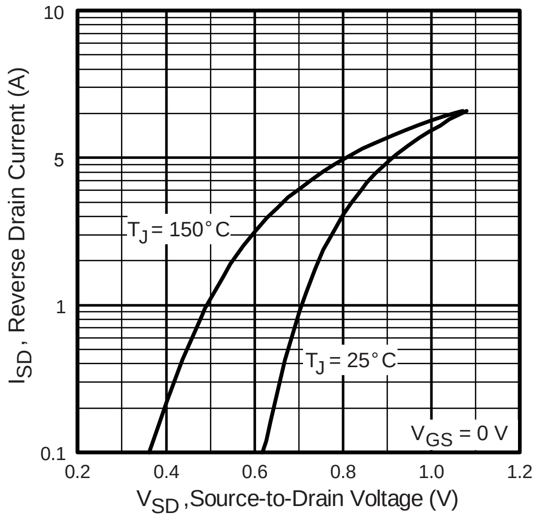


Fig. 7 - Typical Source-Drain Diode Forward Voltage

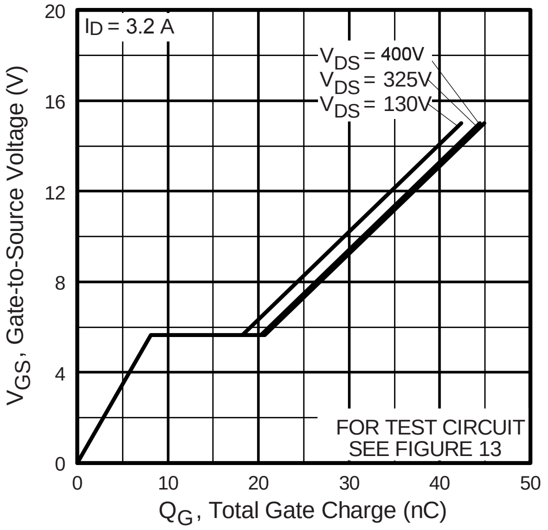


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

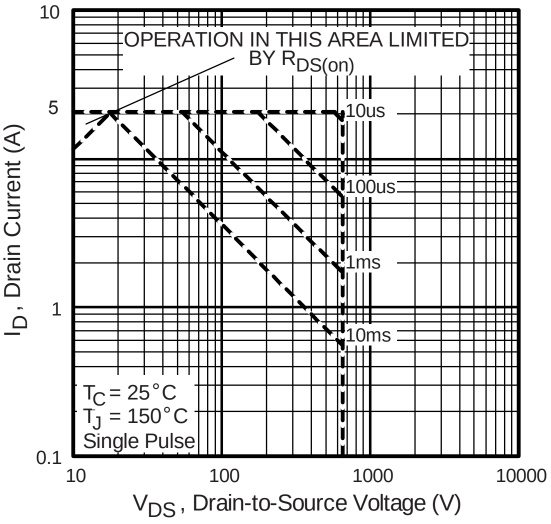


Fig. 8 - Maximum Safe Operating Area

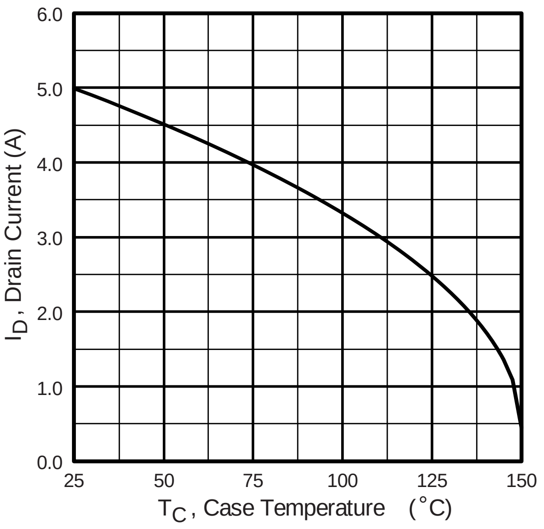


Fig. 9 - Maximum Drain Current vs. Case Temperature

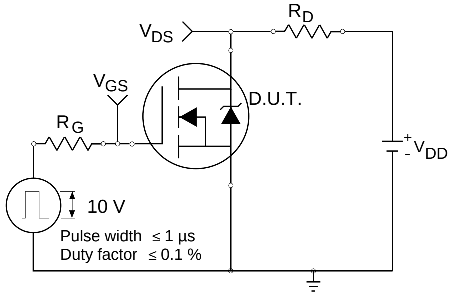


Fig. 10a - Switching Time Test Circuit

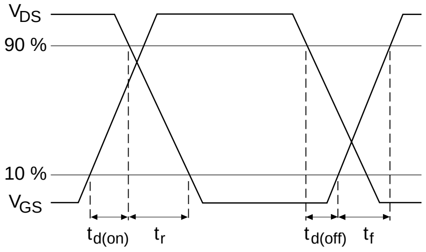


Fig. 10b - Switching Time Waveforms

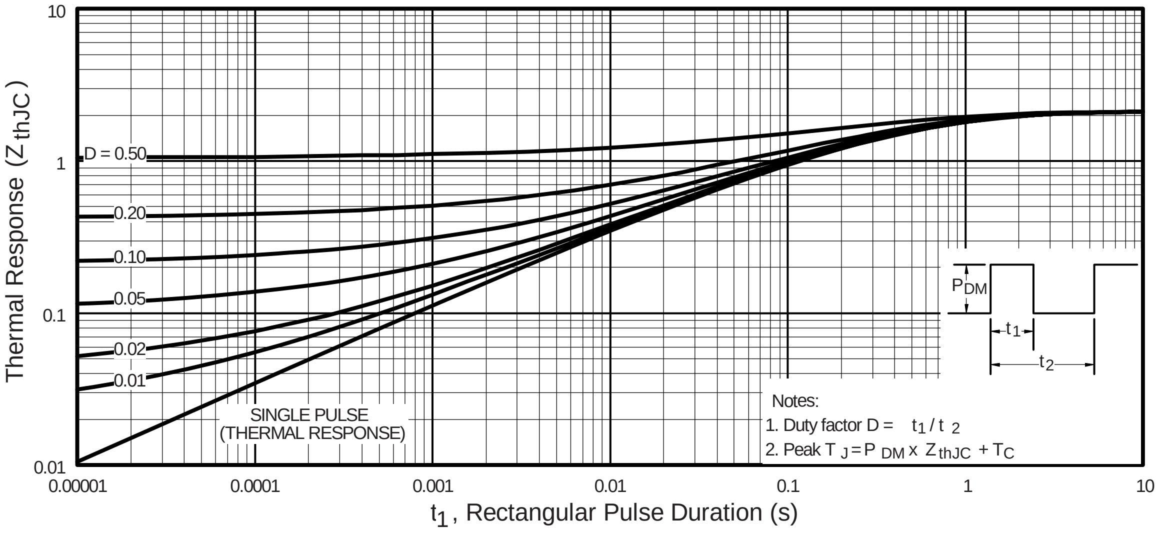


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

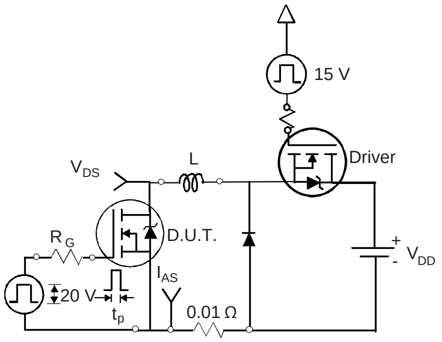


Fig. 12a - Unclamped Inductive Test Circuit

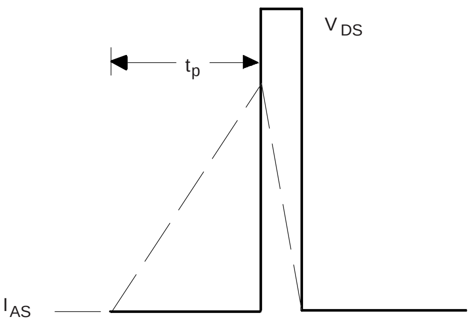


Fig. 12b - Unclamped Inductive Waveforms

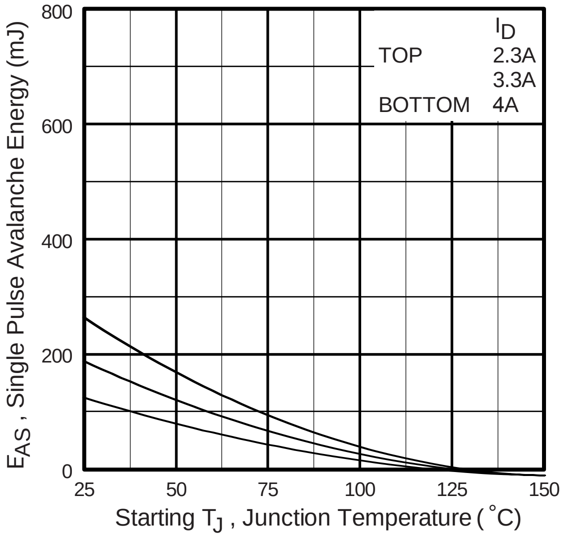


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

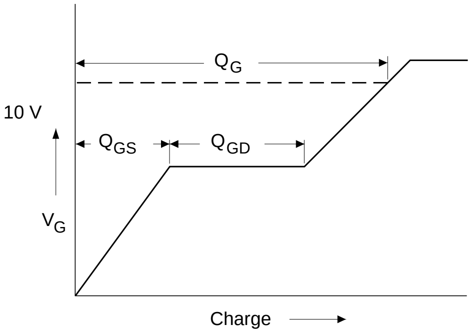


Fig. 13a - Basic Gate Charge Waveform

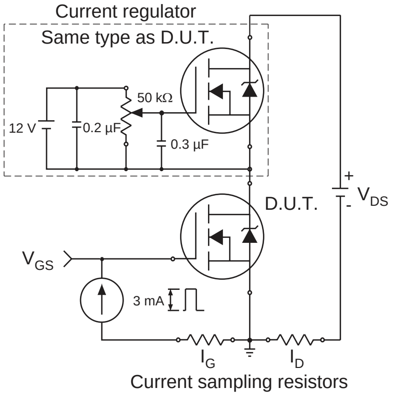


Fig. 13b - Gate Charge Test Circuit

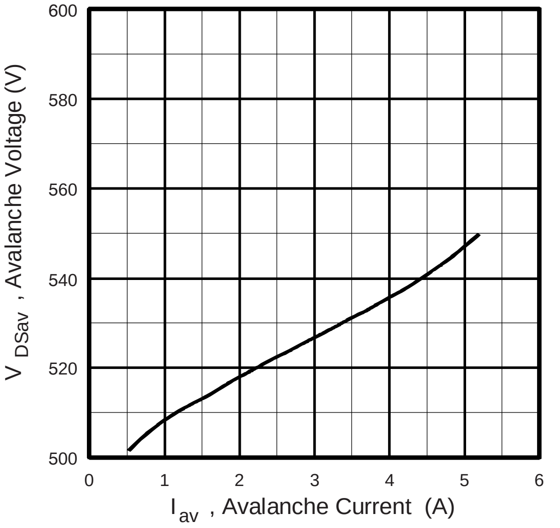
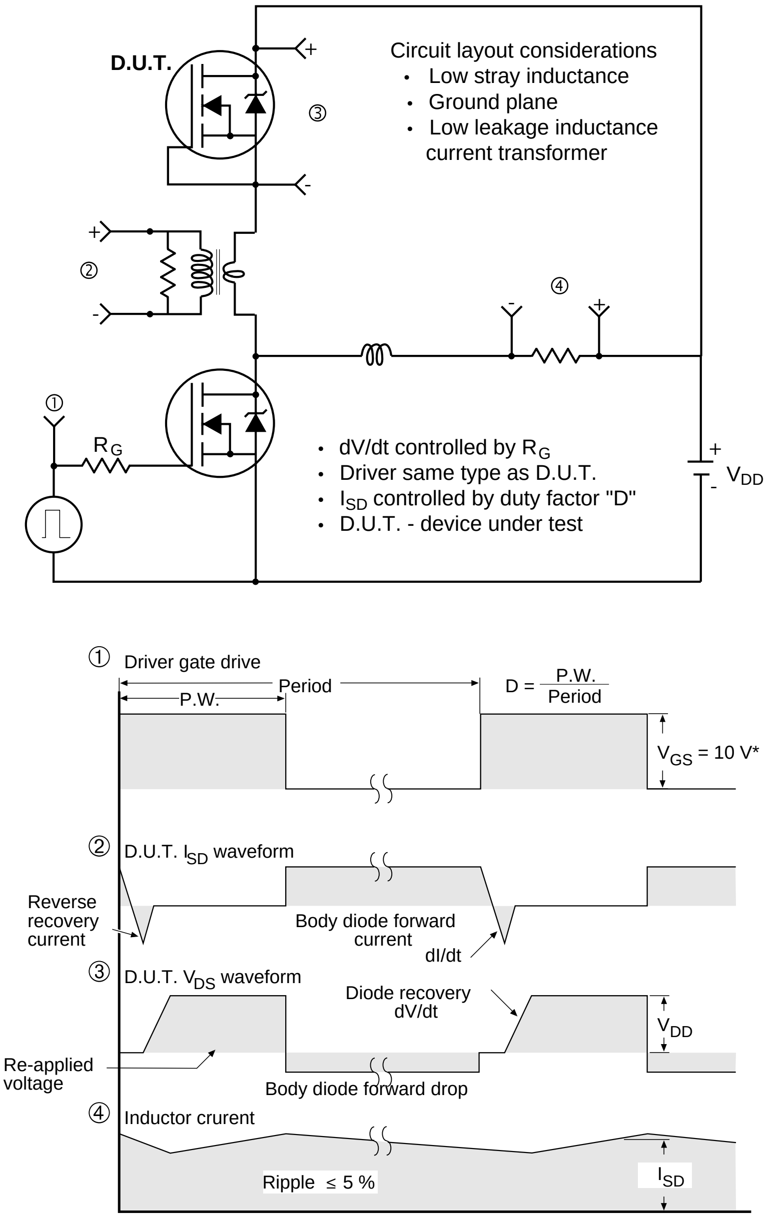


Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current

Peak Diode Recovery dV/dt Test Circuit



Circuit layout considerations
- Low stray inductance
- Ground plane
- Low leakage inductance current transformer

- dV/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by duty factor "D"
- D.U.T. - device under test

* V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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