

## N-Channel 650V (D-S) 175 °C MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V) at T <sub>J</sub> max.	700	
R <sub>DS(on)</sub> max. at 25 °C (Ω)	V <sub>GS</sub> = 10 V	1.3
Q <sub>g</sub> max. (nC)	48	
Q <sub>gs</sub> (nC)	6	
Q <sub>gd</sub> (nC)	11	
Configuration	Single	

### FEATURES

- Low Figure-of-Merit (FOM) R<sub>on</sub> × Q<sub>g</sub>
- Low Input Capacitance (C<sub>iss</sub>)
- Reduced Switching and Conduction Losses
- Ultra Low Gate Charge (Q<sub>g</sub>)
- Avalanche Energy Rated (UIS)

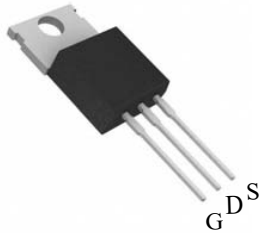


RoHS

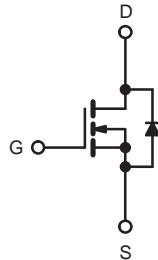
### APPLICATIONS

- Server and Telecom Power Supplies
- Switch Mode Power Supplies (SMPS)
- Power Factor Correction Power Supplies (PFC)
- Lighting
  - High-Intensity Discharge (HID)
  - Fluorescent Ballast Lighting

TO-220 Pin Configuration



Top View




N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	650	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Gate-Source Voltage AC (f > 1 Hz)		30	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	A
		T <sub>C</sub> = 100 °C	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	18	
Linear Derating Factor		0.63	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	56	mJ
Maximum Power Dissipation	P <sub>D</sub>	78	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Drain-Source Voltage Slope	dV/dt	T <sub>J</sub> = 125 °C	V/ns
Reverse Diode dV/dt <sup>d</sup>		27	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s	300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 28.2 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 2 A.
- 1.6 mm from case.
- I<sub>SD</sub> ≤ I<sub>D</sub>, dI/dt = 100 A/μs, starting T<sub>J</sub> = 25 °C.

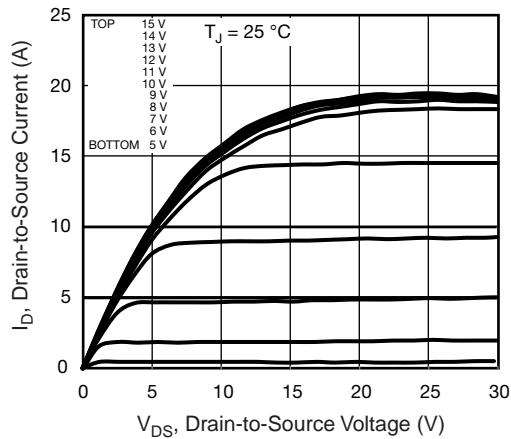
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.6	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		650	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.73	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	-	4	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$	-	0.9	1.3	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 30\text{ V}, I_D = 3\text{ A}$		-	2	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$		-	820	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	40	-	
Reverse Transfer Capacitance	$C_{rss}$			-	4	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$		-	36	-	$\mu\text{F}$
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$			-	117	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}, V_{DS} = 520\text{ V}$	-	24	48	nC
Gate-Source Charge	$Q_{gs}$			-	6	-	
Gate-Drain Charge	$Q_{gd}$			-	11	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}, I_D = 3\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	14	28	ns
Rise Time	$t_r$			-	12	24	
Turn-Off Delay Time	$t_{d(off)}$			-	30	60	
Fall Time	$t_f$			-	20	40	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{ open drain}$		-	1.4	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	7	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	18	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 3\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.3	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 3\text{ A},$ $dI/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	237	-	ns
Reverse Recovery Charge	$Q_{rr}$			-	2.2	-	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	16	-	A

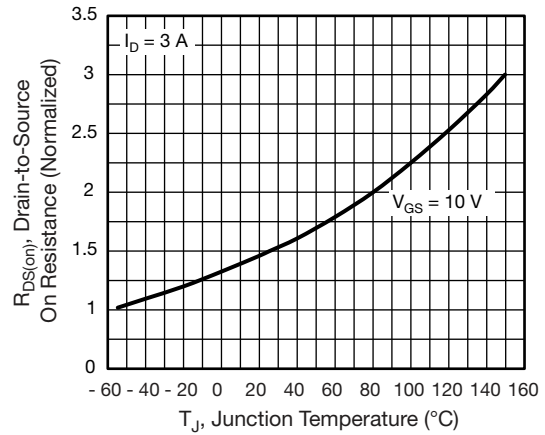
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .
- b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

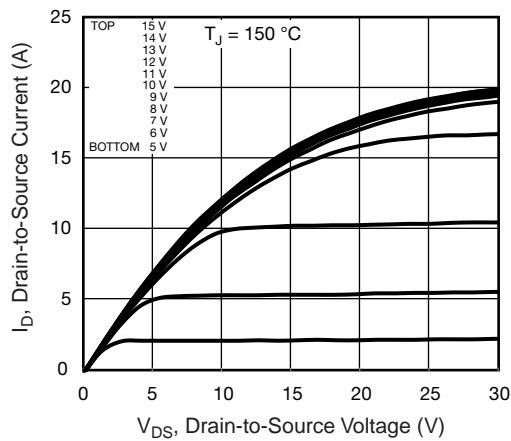
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



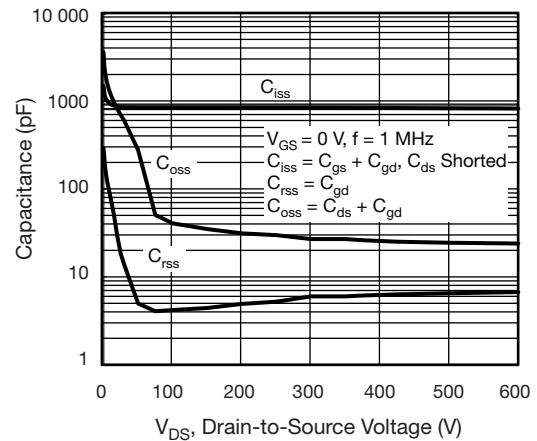
**Fig. 1 - Typical Output Characteristics**



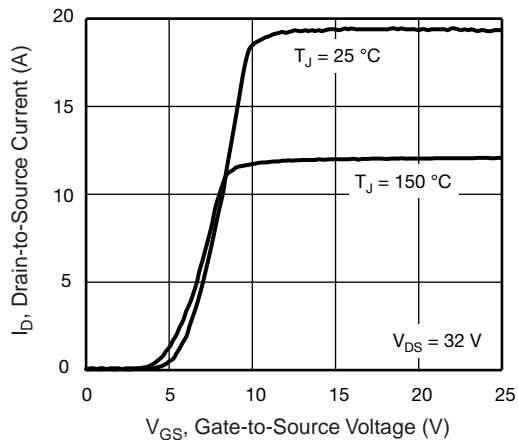
**Fig. 4 - Normalized On-Resistance vs. Temperature**



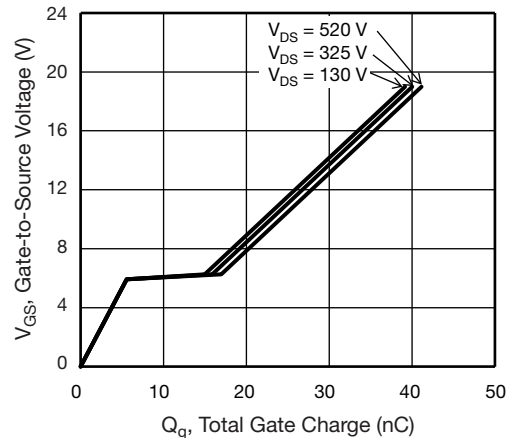
**Fig. 2 - Typical Output Characteristics**



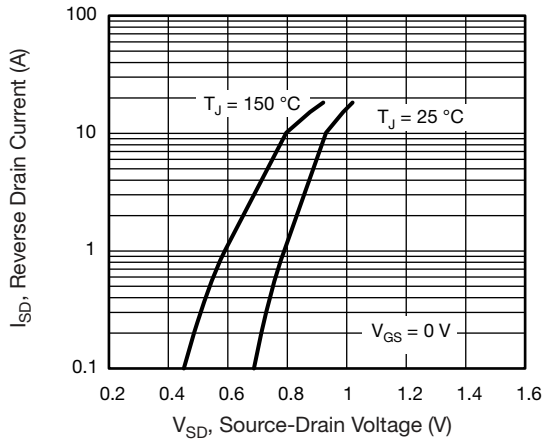
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



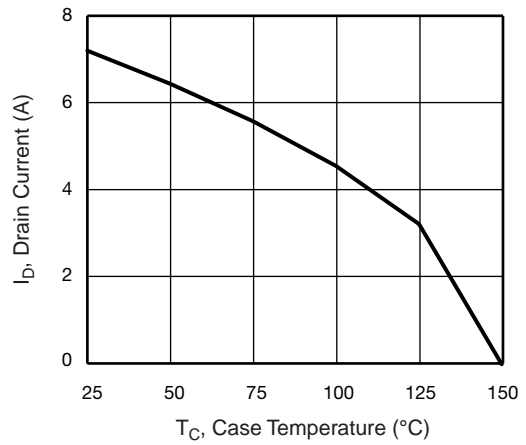
**Fig. 3 - Typical Transfer Characteristics**



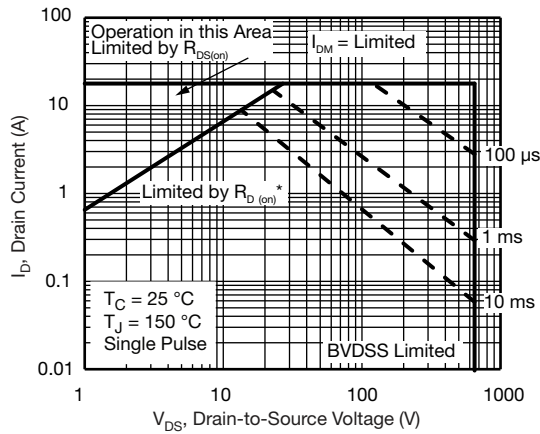
**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

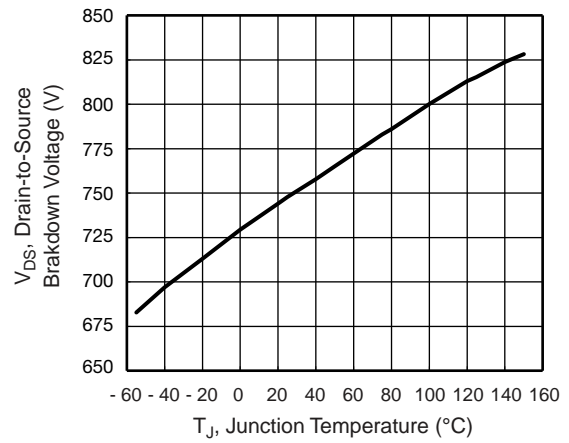


**Fig. 9 - Maximum Drain Current vs. Case Temperature**

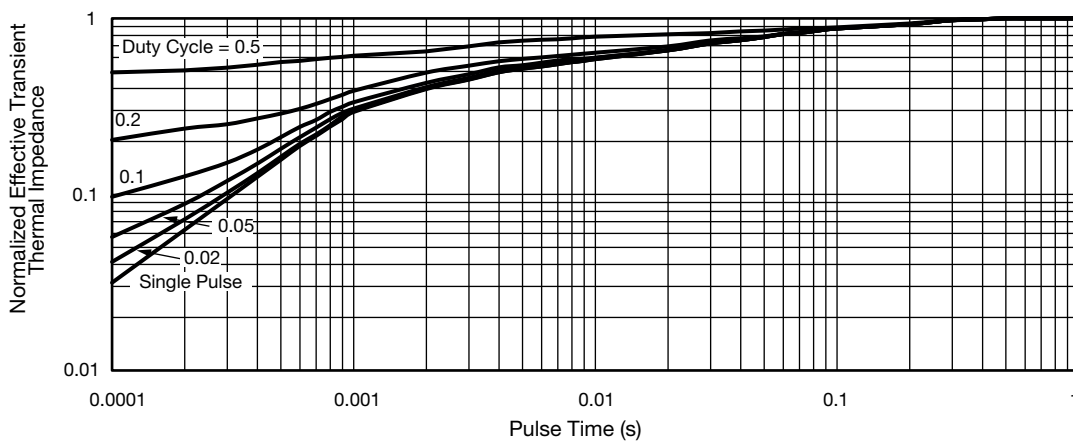


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

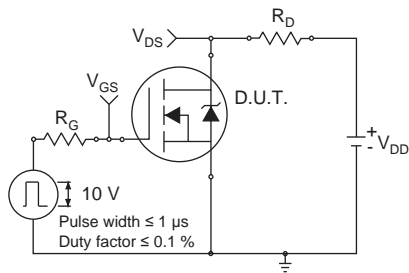
**Fig. 8 - Maximum Safe Operating Area**



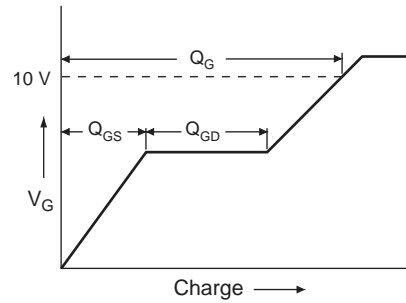
**Fig. 10 - Temperature vs. Drain-to-Source Voltage**



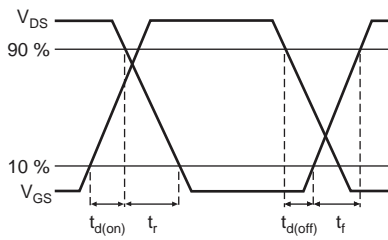
**Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case**



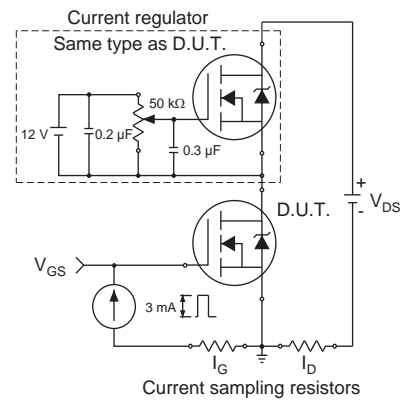
**Fig. 12 - Switching Time Test Circuit**



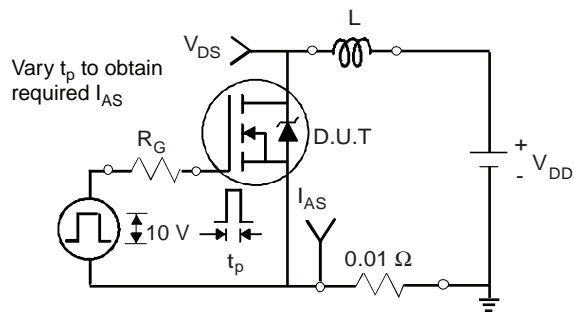
**Fig. 16 - Basic Gate Charge Waveform**



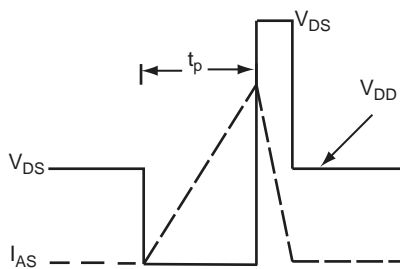
**Fig. 13 - Switching Time Waveforms**



**Fig. 17 - Gate Charge Test Circuit**

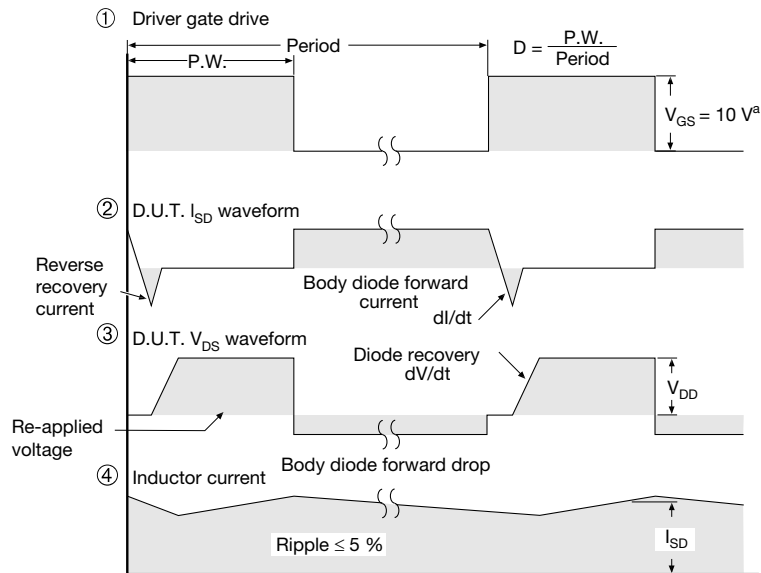
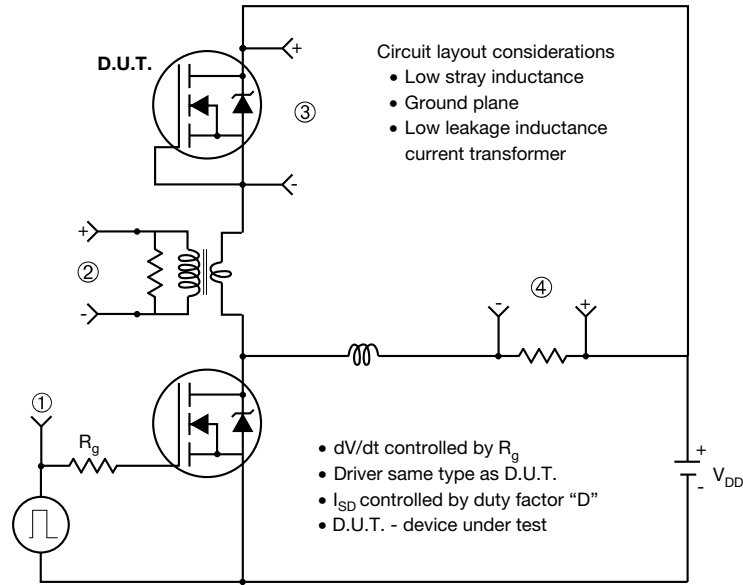


**Fig. 14 - Unclamped Inductive Test Circuit**



**Fig. 15 - Unclamped Inductive Waveforms**

**Peak Diode Recovery dV/dt Test Circuit**

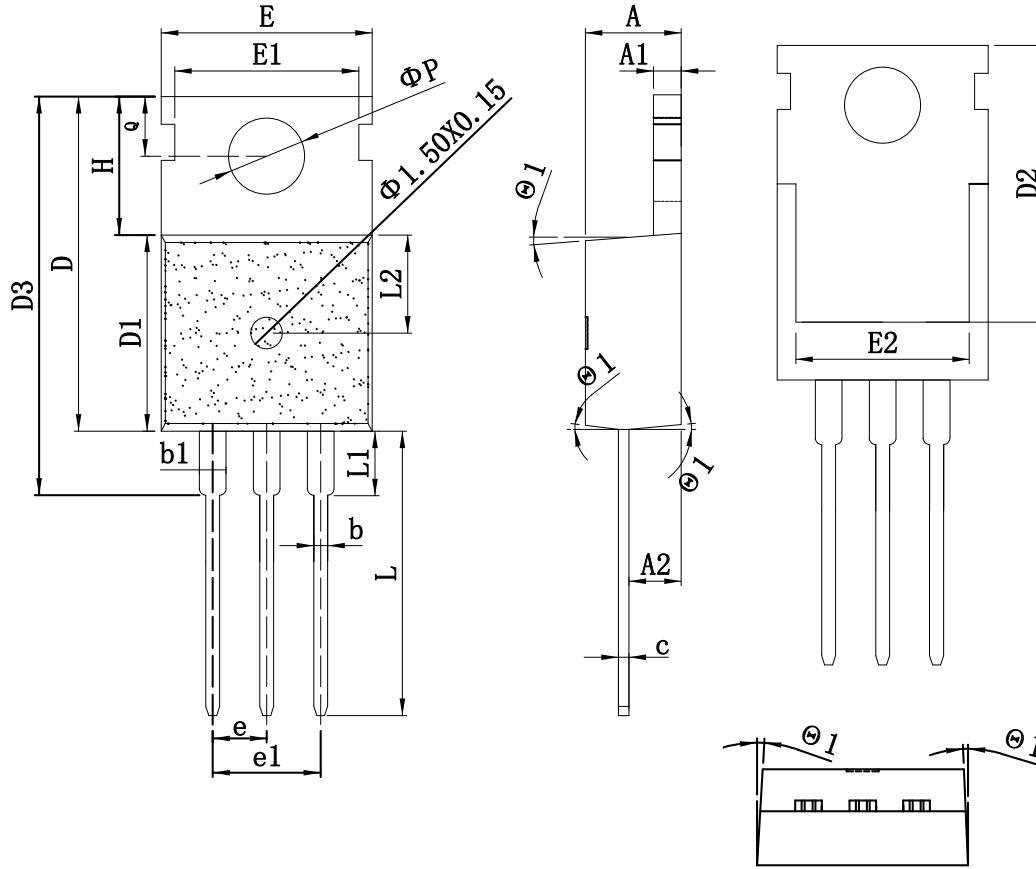


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 18 - For N-Channel**

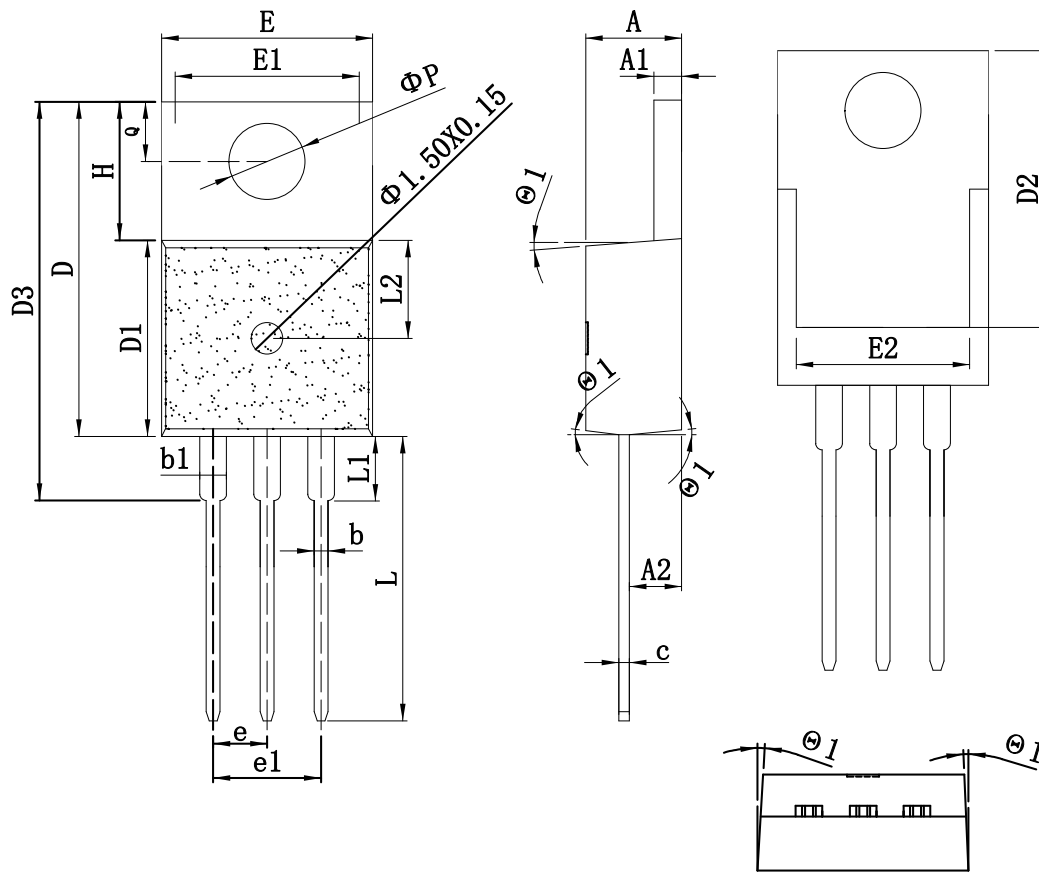
**TO-220\_3L-A PACKAGE OUTLINE**



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	mm			SYMBOL	mm		
	MIN	TYP	MAX		MIN	TYP	MAX
A	4.15	4.50	4.80	E1	8.25	8.70	9.15
A1	1.15	1.30	1.50	E2	7.20	8.00	8.80
A2	2.10	2.40	2.65	e	2.38	2.54	2.74
b	0.65	0.80	1.00	e1	5.08REF		
b1	1.10	1.33	1.80	H	6.20	6.50	6.90
c	0.35	0.50	0.65	L	12.75	13.28	13.70
D	14.25	15.75	16.15	L1	-	-	3.50
D1	8.70	9.20	9.60	L2	2.30	4.65	7.00
D2	12.30	13.10	13.85	φP	3.40	3.65	3.85
D3	16.20	18.80	20.60	Q	2.50	2.80	3.00
E	8.68	10.02	11.00	θ	2°	-	7°

### TO-220\_3L-B PACKAGE OUTLINE



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	mm			SYMBOL	mm		
	MIN	TYP	MAX		MIN	TYP	MAX
A	4.15	4.50	4.80	E1	8.25	8.70	9.15
A1	1.15	1.30	1.50	E2	7.20	8.00	8.80
A2	2.10	2.40	2.65	e	2.38	2.54	2.74
b	0.65	0.80	1.00	e1	5.08REF		
b1	1.10	1.33	1.80	H	6.20	6.50	6.90
c	0.35	0.50	0.65	L	12.75	13.28	13.70
D	14.25	15.75	16.15	L1	-	-	3.50
D1	8.70	9.20	9.60	L2	2.30	4.65	7.00
D2	12.30	13.10	13.85	$\phi P$	3.40	3.65	3.85
D3	16.20	18.80	20.60	Q	2.50	2.80	3.00
E	8.68	10.02	11.00	$\theta$	2°	-	7°



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