

P-Channel 150-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 150	0.8at $V_{GS} = - 10$ V	- 4.5 A	6.8 nC

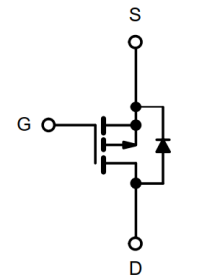
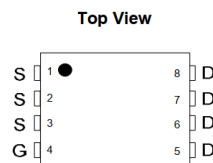
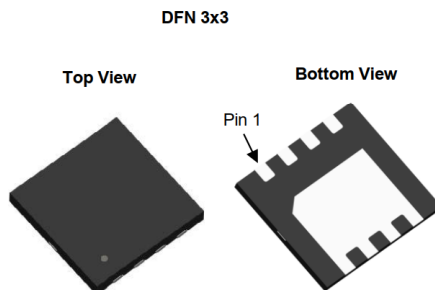
FEATURES

- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested


RoHS
COMPLIANT

APPLICATIONS

- Low On Resistance
- Low Gate Charge
- Fast Switching Characteristic



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 150	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	- 4.5 ^a	A
	$T_C = 100$ °C	- 2.9 ^a	
	$T_A = 25$ °C	- 1.2 ^{b, c}	
	$T_A = 70$ °C	- 0.8 ^{b, c}	
Pulsed Drain Current	I_{DM}	- 18.5	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	- 4.5 ^a	
	$T_A = 25$ °C	- 1.2 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	- 9	
Single Pulse Avalanche Energy	E_{AS}	3.5	mJ
Maximum Power Dissipation	$T_C = 25$ °C	45	W
	$T_C = 100$ °C	18	
	$T_A = 25$ °C	2.5 ^{b, c}	
	$T_A = 70$ °C	1.6 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	50	-	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	2.8	-	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. The DFN3x3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 54 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-150			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-39		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			6.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-2.0		-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -120\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -120\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	-4.5			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -1.5\text{ A}$		0.8	1.4	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -1.5\text{ A}$		2.7		S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{DS} = -75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		288		pF
Output Capacitance	C_{oss}			76		
Reverse Transfer Capacitance	C_{rss}			25		
Total Gate Charge	Q_g	$V_{DS} = -75\text{ V}, V_{GS} = -10\text{ V}, I_D = -1.5\text{ A}$		6.8		nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			3.2		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.6		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = -75\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong -1.5\text{ A}, V_{GS} = -10\text{ V}, R_g = 1\text{ }\Omega$		10		ns
Rise Time	t_r			22		
Turn-Off Delay Time	$t_{d(off)}$			28		
Fall Time	t_f			15		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-4.5	A
Pulse Diode Forward Current ^a	I_{SM}				-18.5	
Body Diode Voltage	V_{SD}	$I_S = -1.5\text{ A}$		-0.7	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -1.5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		40		ns
Body Diode Reverse Recovery Charge	Q_{rr}			75		nC
Reverse Recovery Fall Time	t_a			19		ns
Reverse Recovery Rise Time	t_b			14		

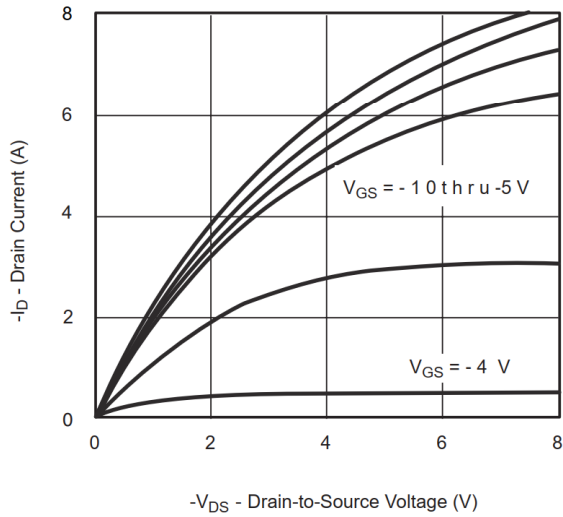
Notes:

 a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

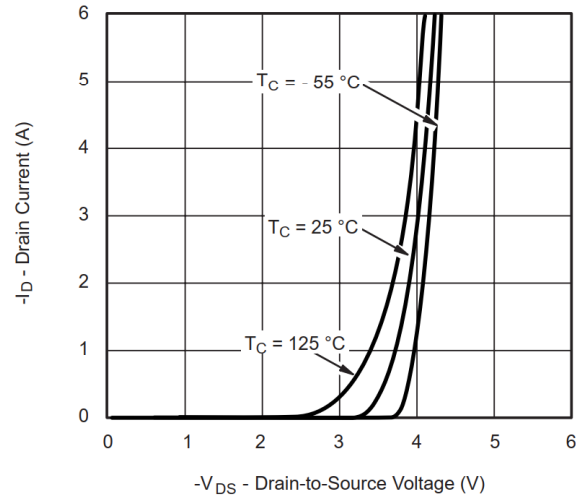
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

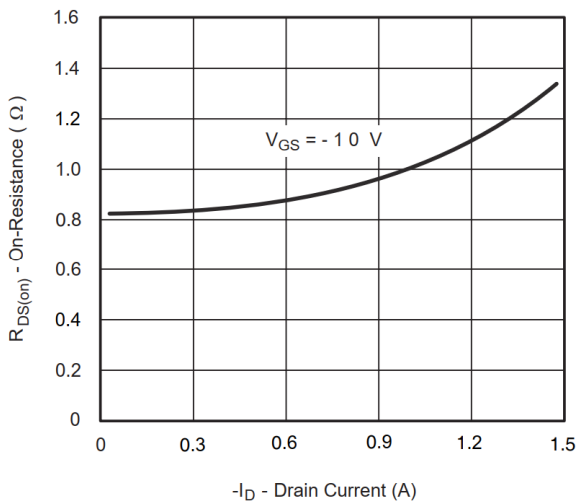
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



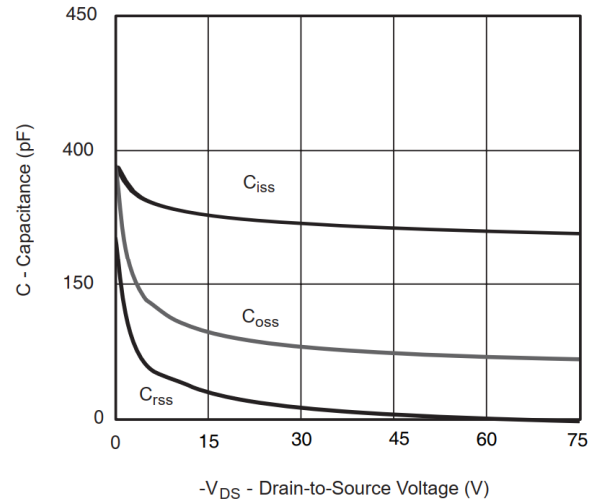
Output Characteristics



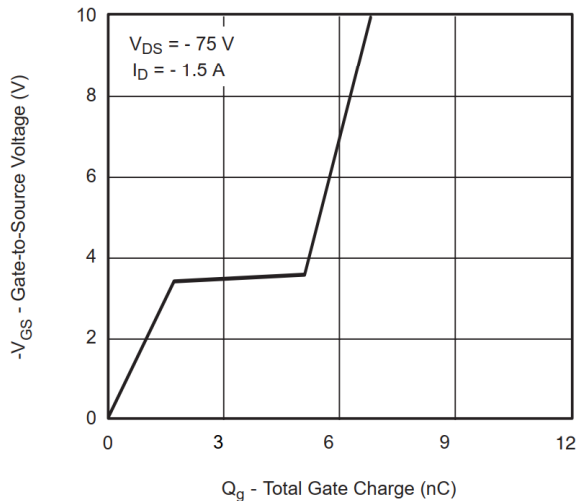
Transfer Characteristics



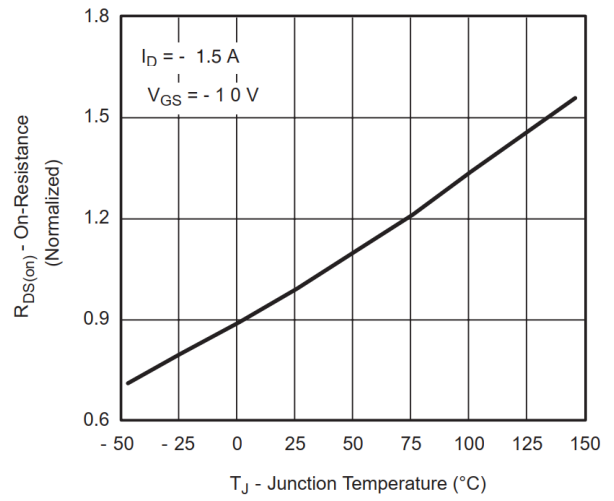
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

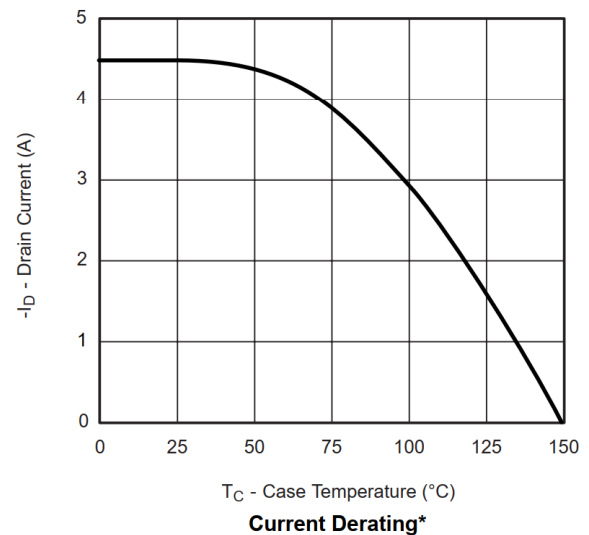
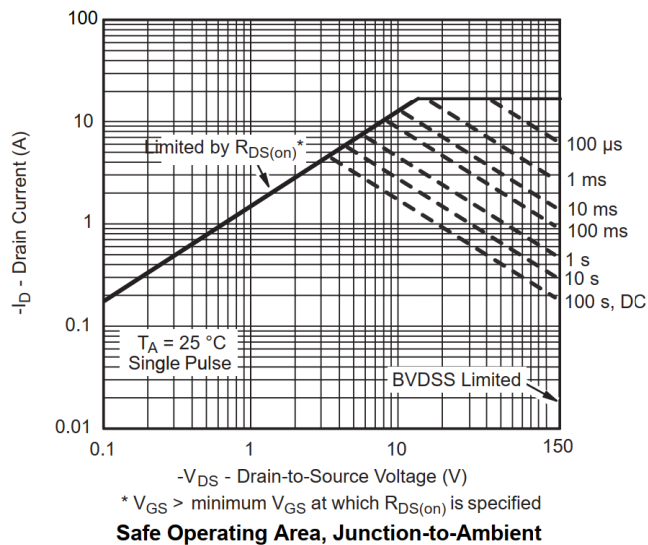
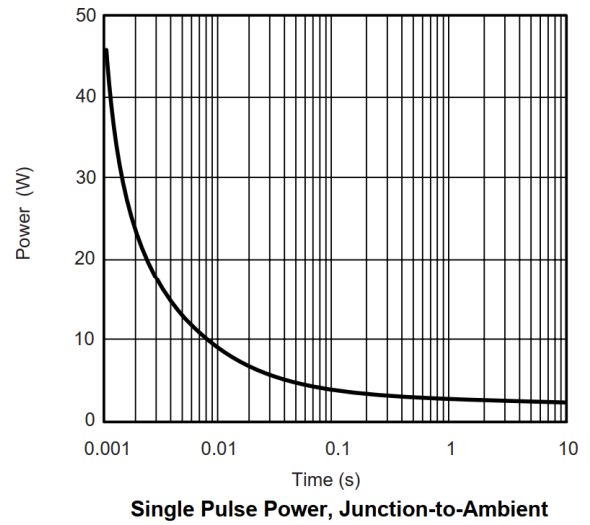
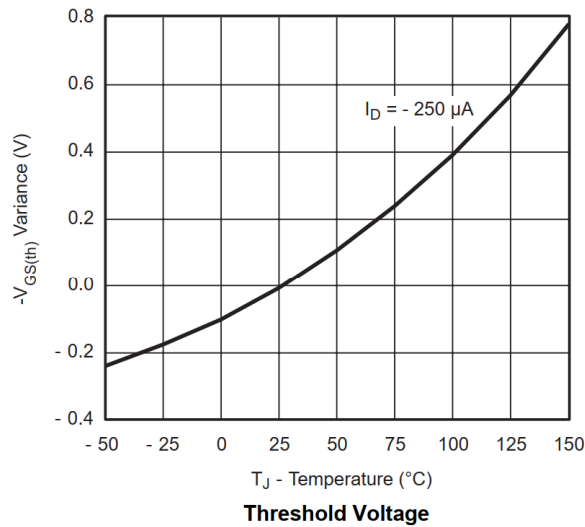
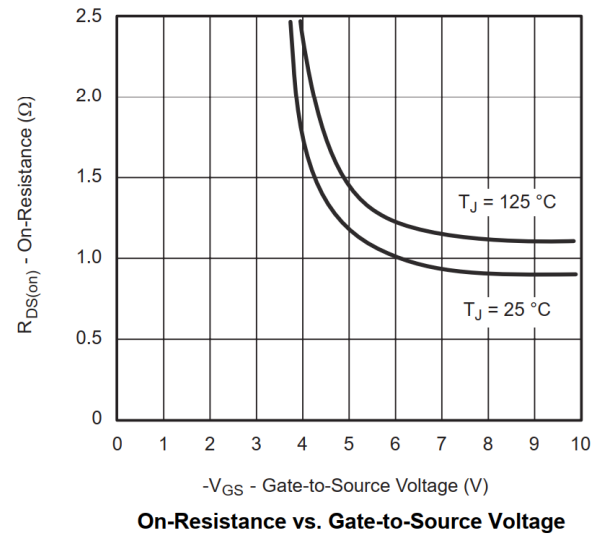
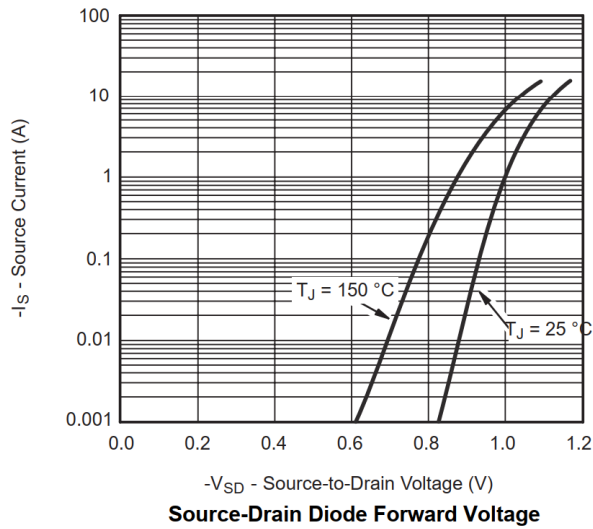


Gate Charge

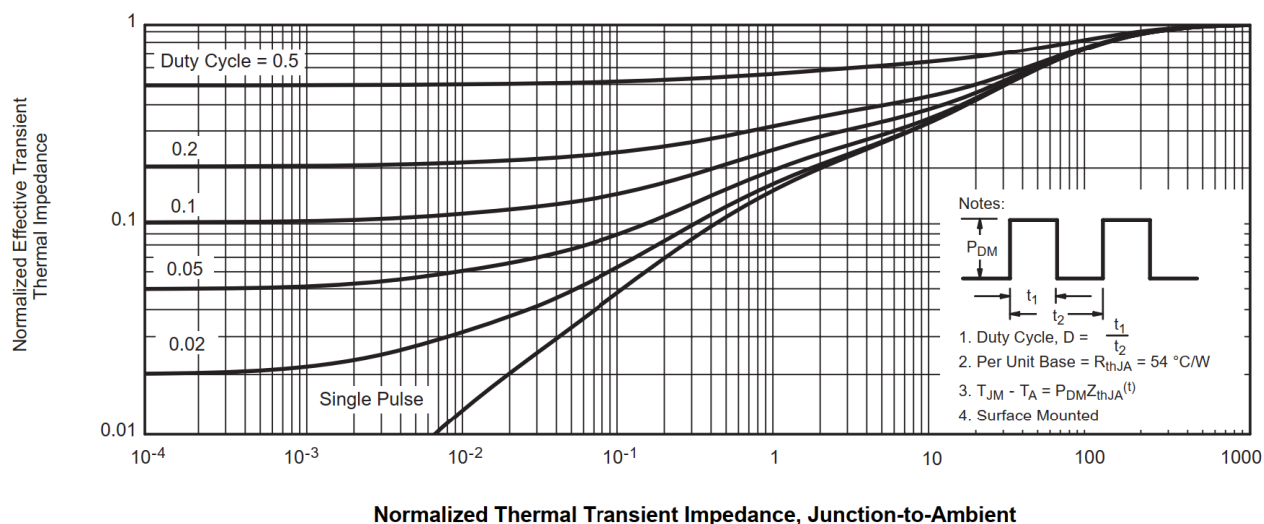


On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

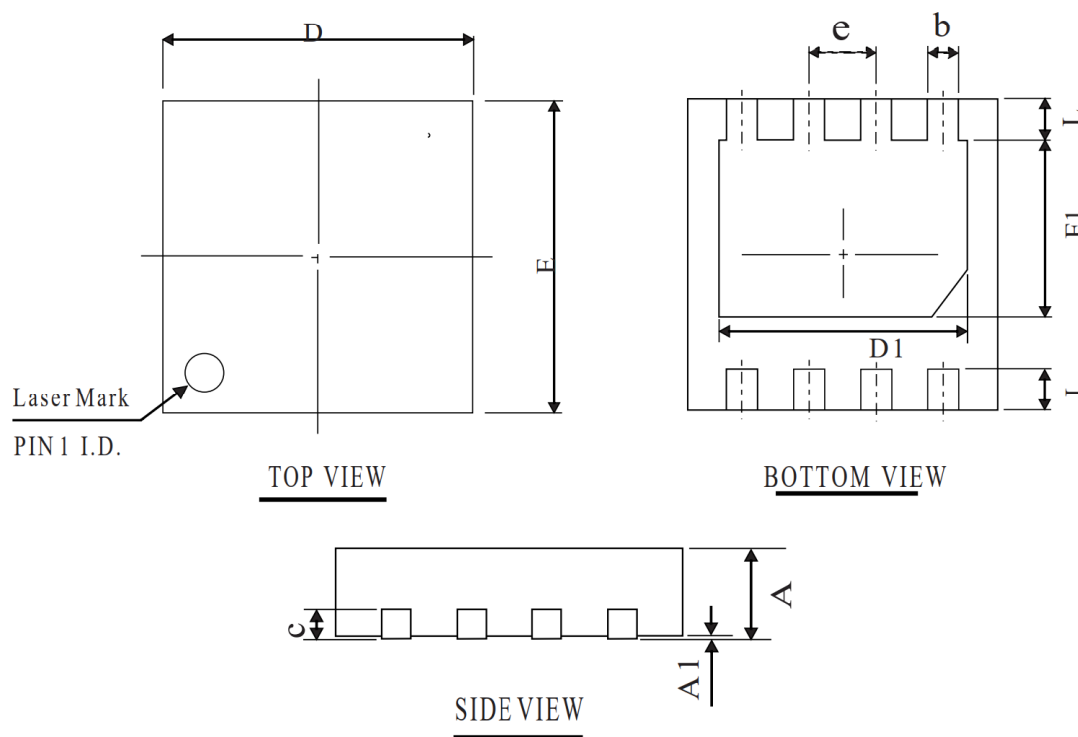


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

DFN3*3-8L PACKAGE OUTLINE



COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	0.60	0.75	0.90
A1	0.00	0.02	0.08
b	0.20	0.30	0.45
D	2.85	3.00	3.15
E	2.85	3.00	3.15
D1	2.10	2.40	2.70
E1	1.50	1.70	2.00
L	0.20	0.40	0.60
c	0.203 REF		
e	0.65 BSC		

OTHER DIMENSIONS

A	0.50	0.55	0.60
A	0.40	0.45	0.50

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