

N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ.)
60	0.0072 at V _{GS} = 10 V	48	9nC
	0.0098 at V _{GS} = 4.5 V	33	

FEATURES

- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested

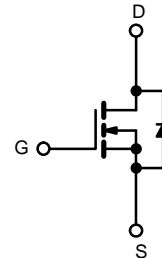
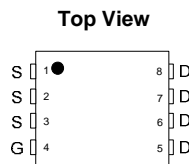
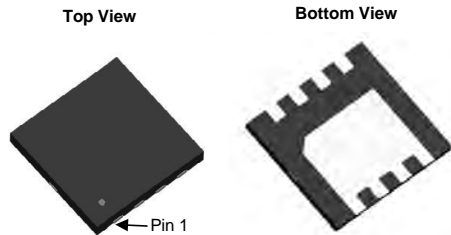


RoHS
COMPLIANT

APPLICATIONS

- Notebook PC Core
- VRM/POL

DFN 3x3 EP



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 175 °C)	I _D	T _C = 25 °C	48 ^{a, e}	A
		T _C = 70 °C	40 ^e	
		T _A = 25 °C	16 ^{b, c}	
		T _A = 70 °C	9 ^{b, c}	
Pulsed Drain Current	I _{DM}	192		
Avalanche Current Pulse	L = 0.1 mH	I _{AS}	45	
Single Pulse Avalanche Energy		E _{AS}	51	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	35	W
		T _C = 70 °C	22.4	
		T _A = 25 °C	3.1 ^{b, c}	
		T _A = 70 °C	1.98 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	32	45	°C/W
Maximum Junction-to-Case	R _{thJC}	2.6	4.5	

Notes:

a. Based on T_C = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under steady state conditions is 90 °C/W.

e. Calculated based on maximum junction temperature. Package limitation current is 80 A.

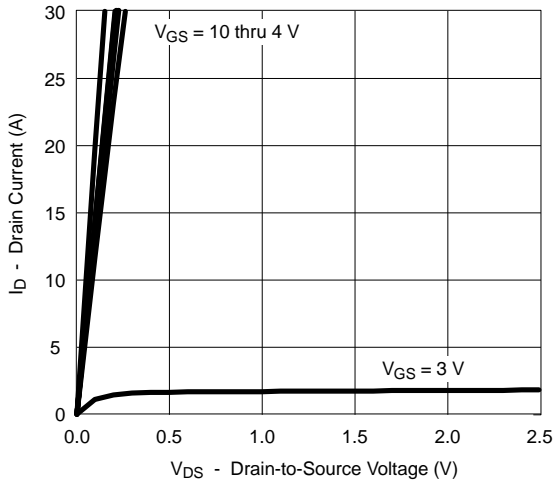
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min .	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		3.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	56			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$		0.0072	0.0089	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$		0.0098	0.012	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 48\text{ V}, I_D = 12\text{ A}$		87		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2510		pF
Output Capacitance	C_{oss}			298		
Reverse Transfer Capacitance	C_{rss}			95		
Total Gate Charge	Q_g	$V_{DS} = 48\text{ V}, V_{GS} = 10\text{ V}, I_D = 12\text{ A}$		16		nC
		$V_{DS} = 48\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$		9		
Gate-Source Charge	Q_{gs}	$V_{DS} = 48\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$		5		
Gate-Drain Charge	Q_{gd}			4		
Gate Resistance	R_g		$f = 1\text{ MHz}$		1.4	2.2
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 48\text{ V}, R_L = 0.555\text{ }\Omega$ $I_D \cong 7\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		18	29	ns
Rise Time	t_r			11	19	
Turn-Off Delay Time	$t_{d(off)}$			70	115	
Fall Time	t_f			10	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 48\text{ V}, R_L = 0.625\text{ }\Omega$ $I_D \cong 4\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		55	87	
Rise Time	t_r			180	273	
Turn-Off Delay Time	$t_{d(off)}$			55	86	
Fall Time	t_f			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			48	A
Pulse Diode Forward Current ^a	I_{SM}				192	
Body Diode Voltage	V_{SD}	$I_S = 12\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		52	78	ns
Body Diode Reverse Recovery Charge	Q_{rr}			70.2	105	nC
Reverse Recovery Fall Time	t_a			27		ns
Reverse Recovery Rise Time	t_b			25		

Notes:

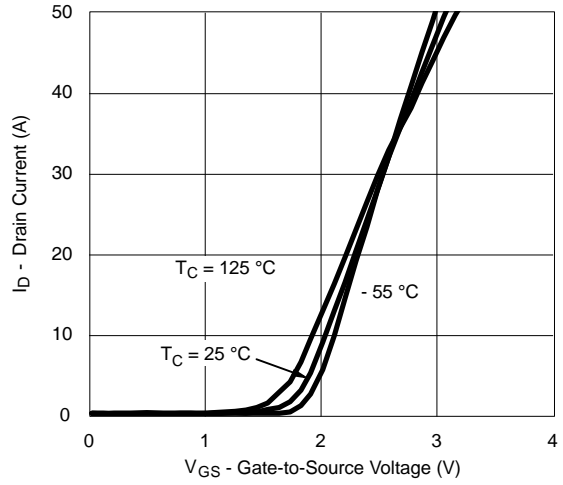
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

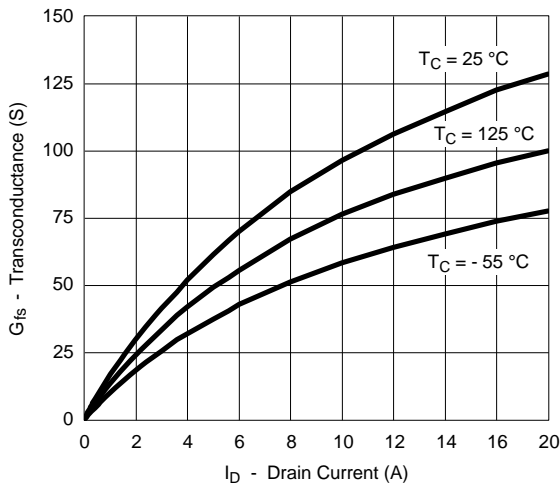
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



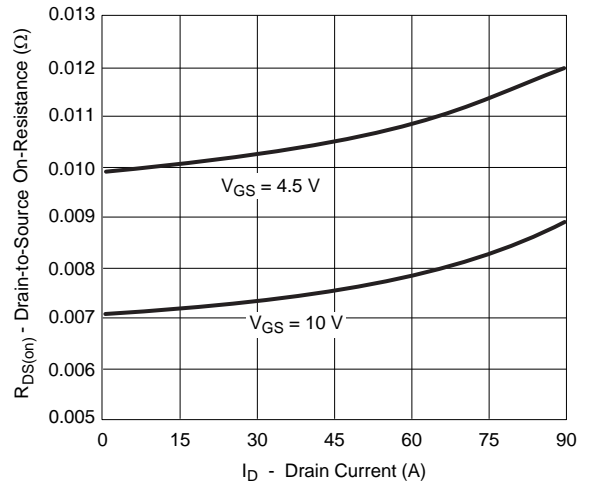
Output Characteristics



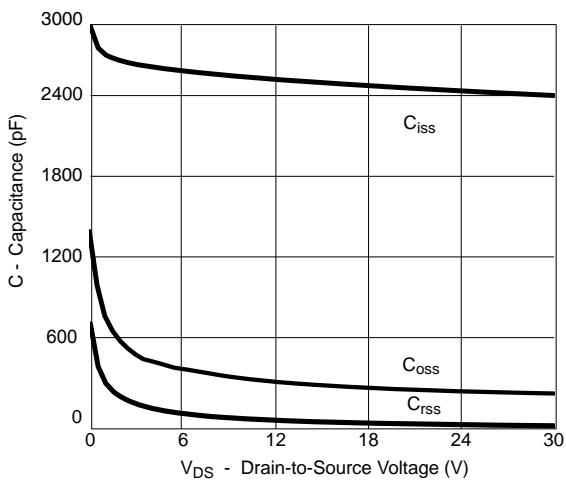
Transfer Characteristics



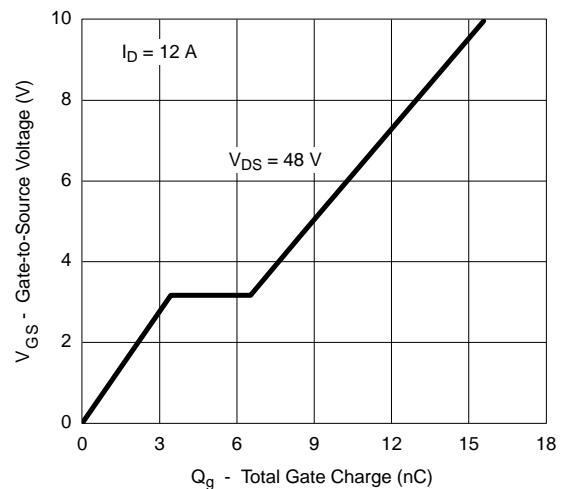
Transconductance



$R_{DS(on)}$ vs. Drain Current

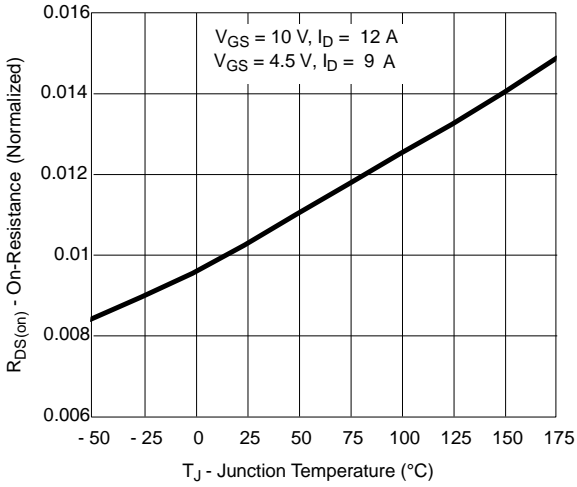


Capacitance



Gate Charge

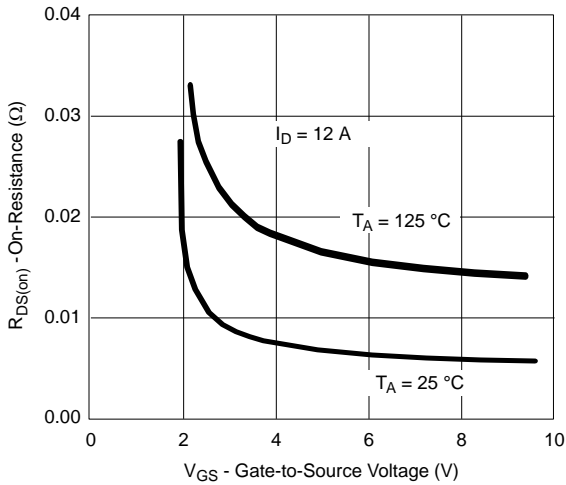
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



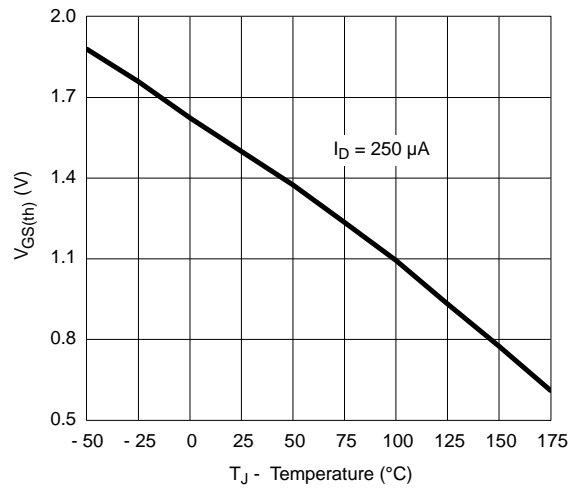
On-Resistance vs. Junction Temperature



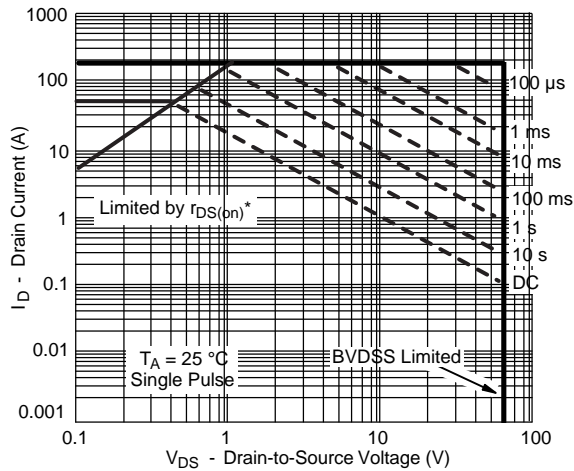
Forward Diode Voltage vs. Temperature



R_{DS(on)} vs. V_{GS} vs. Temperature

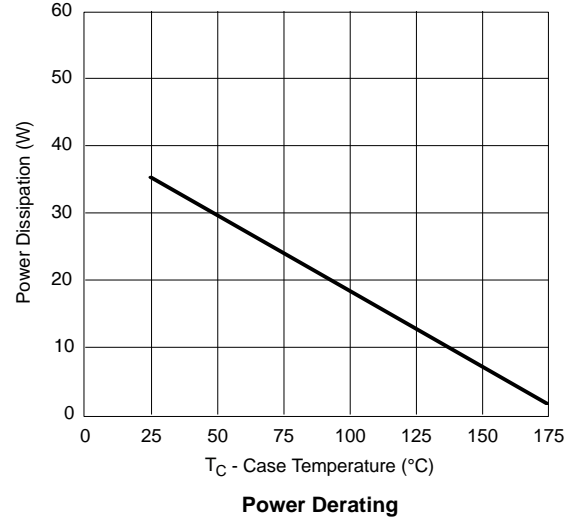
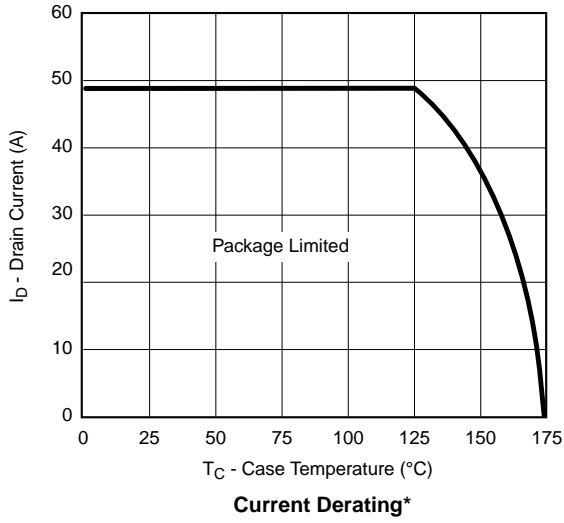


Threshold Voltage

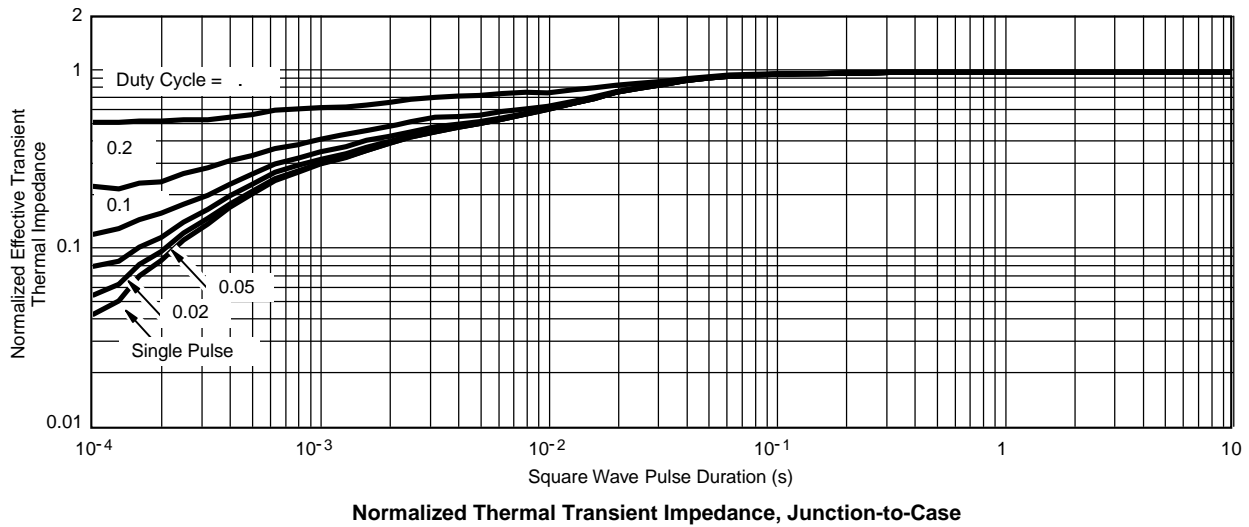


*V_{GS} > minimum V_{GS} at which r_{DS(on)} is specified
Safe Operating Area, Junction-to-Ambient

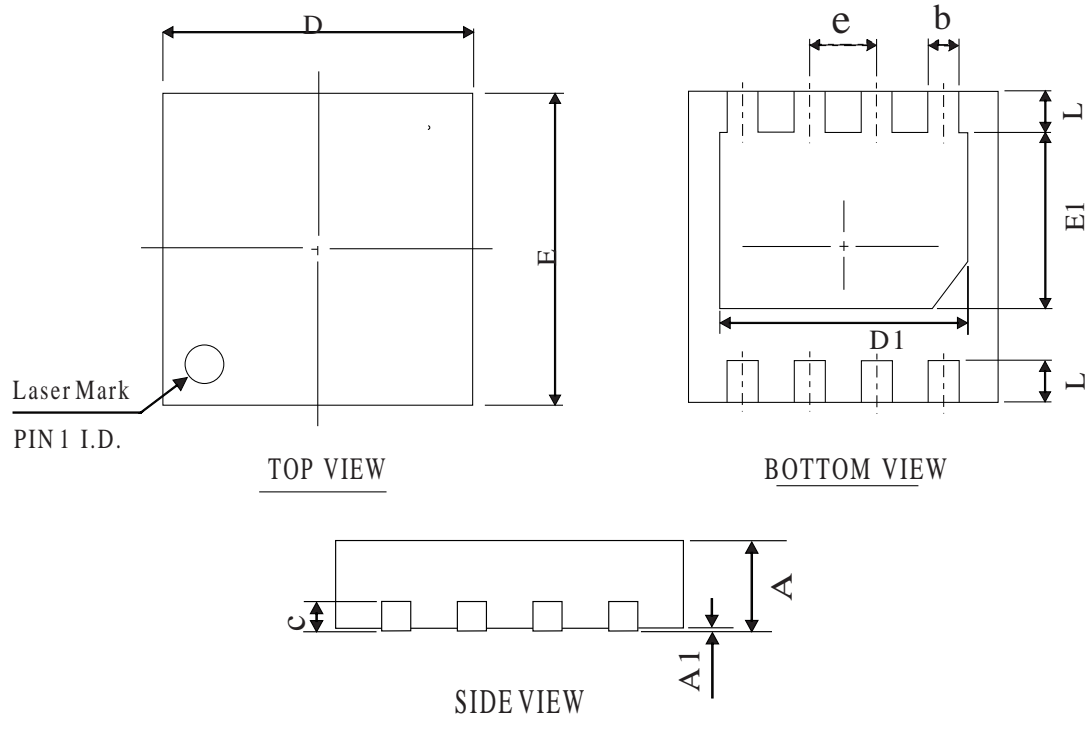
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



DFN3*3-8L PACKAGE OUTLINE



COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	0.60	0.75	0.90
A1	0.00	0.02	0.08
b	0.20	0.30	0.45
D	2.85	3.00	3.15
E	2.85	3.00	3.15
D1	2.10	2.40	2.70
E1	1.50	1.70	2.00
L	0.20	0.40	0.60
C	0.203 REF		
e	0.65 BSC		

OTHER DIMENSIONS

A	0.50	0.55	0.60
A	0.40	0.45	0.50

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