

N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (mΩ)	I _D (A) ^{a, e}	Q _g (Typ.)
80	8 at V _{GS} = 10 V	45	18 nC
	14 at V _{GS} = 4.5 V	30	

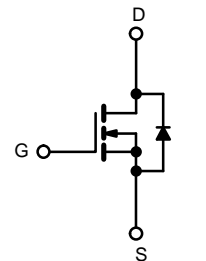
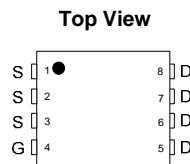
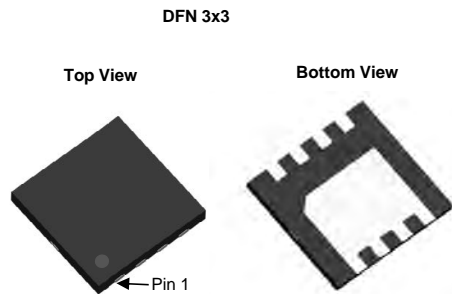
FEATURES

- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested



APPLICATIONS

- Notebook PC Core
- VRM/POL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	80	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 175 °C)	I _D	T _C = 25 °C	45 ^{a, e}	A
		T _C = 70 °C	38 ^e	
		T _A = 25 °C	16 ^{b, c}	
		T _A = 70 °C	9 ^{b, c}	
Pulsed Drain Current	I _{DM}	180		
Avalanche Current Pulse	L = 0.1 mH	I _{AS}	43	mJ
Single Pulse Avalanche Energy		E _{AS}	48	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	45 ^{a, e}	A
		T _A = 25 °C	15 ^{b, c}	
Maximum Power Dissipation	P _D	T _C = 25 °C	56	W
		T _C = 70 °C	35.8	
		T _A = 25 °C	4.2 ^{b, c}	
		T _A = 70 °C	2.69 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	45	60	°C/W	
Maximum Junction-to-Case					

Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under steady state conditions is 90 °C/W.
e. Calculated based on maximum junction temperature.

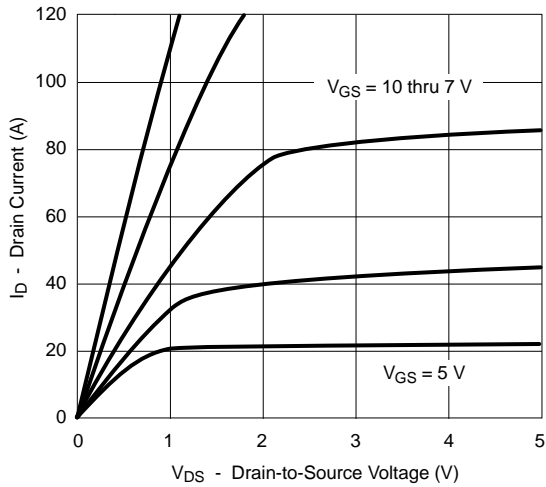
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0		3.6	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	45			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		8	9.8	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		14	20	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 5\text{ V}, I_D = 20\text{ A}$		37		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1010		pF
Output Capacitance	C_{oss}			192		
Reverse Transfer Capacitance	C_{rss}			18		
Total Gate Charge	Q_g	$V_{DS} = 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		18		nC
Gate-Source Charge	Q_{gs}			7.9		
Gate-Drain Charge	Q_{gd}			5		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.4	2.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 0.555\text{ }\Omega$ $I_D \cong 20\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		15		ns
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			20		
Fall Time	t_f			9		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 0.625\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		30		
Rise Time	t_r			22		
Turn-Off Delay Time	$t_{d(off)}$			42		
Fall Time	t_f			12		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			45	A
Pulse Diode Forward Current ^a	I_{SM}				180	
Body Diode Voltage	V_{SD}	$I_S = 20\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		42		ns
Body Diode Reverse Recovery Charge	Q_{rr}			70		nC
Reverse Recovery Fall Time	t_a			29		ns
Reverse Recovery Rise Time	t_b			25		

Notes:

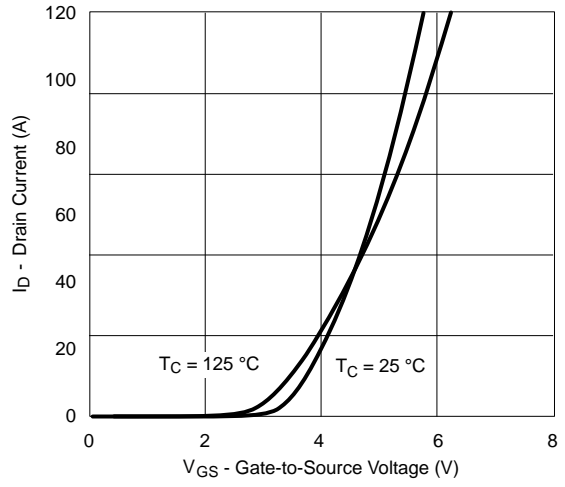
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

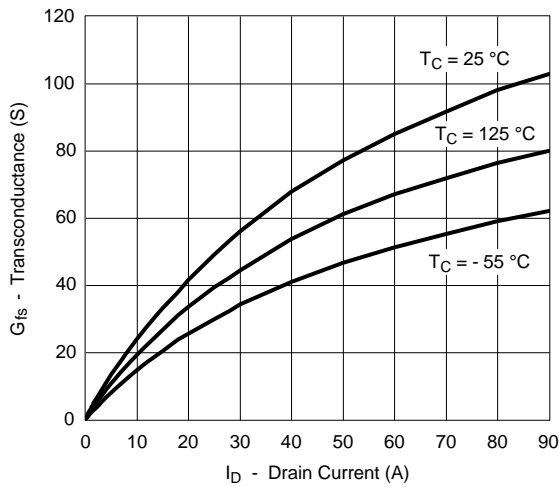
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



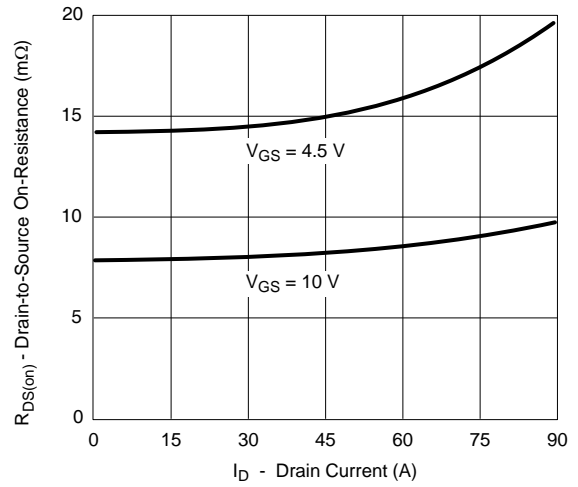
Output Characteristics



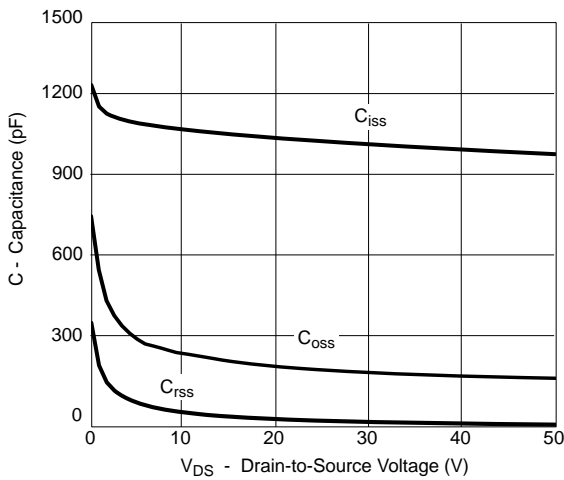
Transfer Characteristics



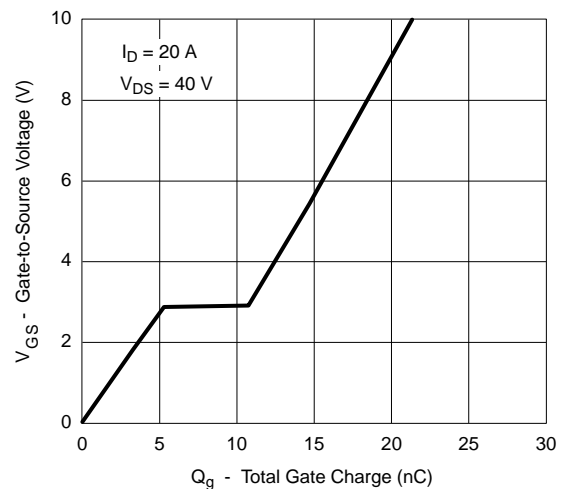
Transconductance



$R_{DS(on)}$ vs. Drain Current

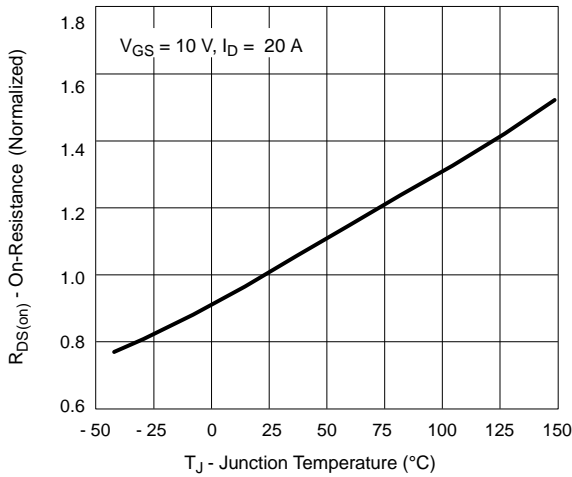


Capacitance

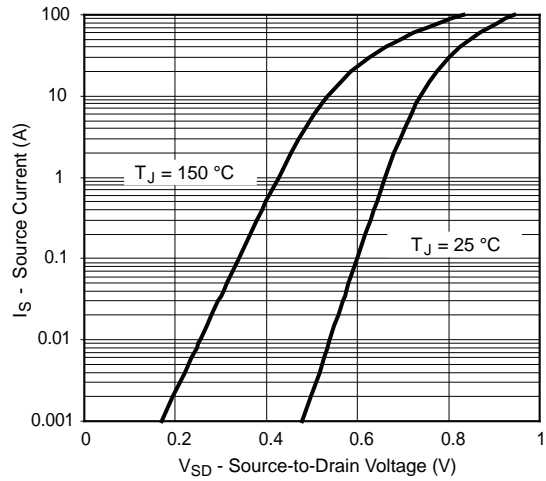


Gate Charge

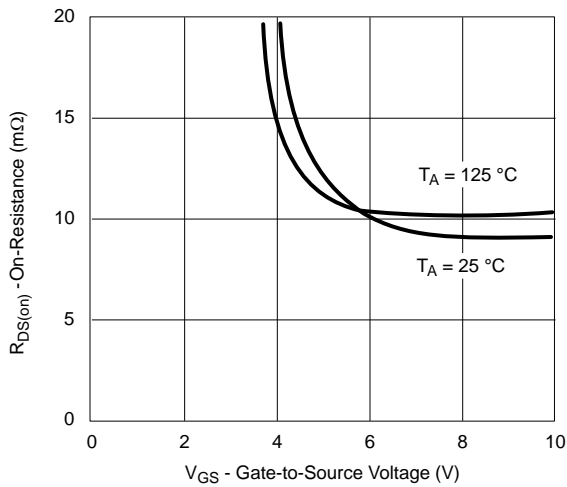
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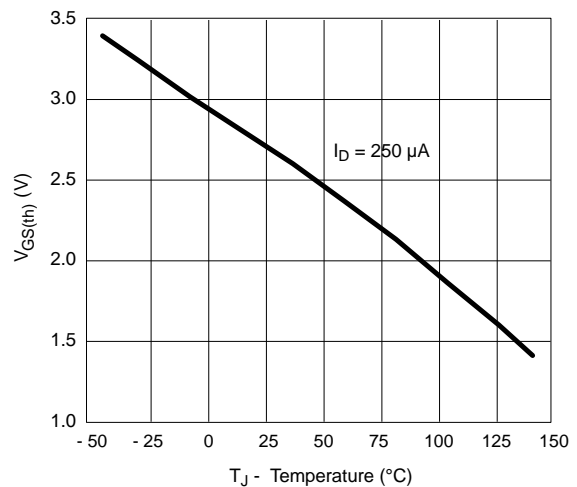
On-Resistance vs. Junction Temperature



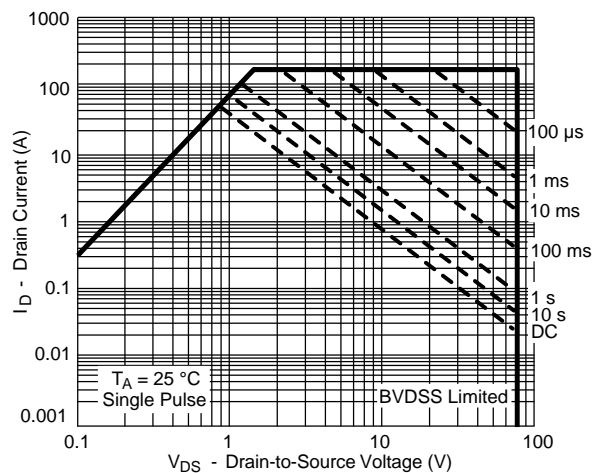
Forward Diode Voltage vs. Temperature



R_{DS(on)} vs. V_{GS} vs. Temperature

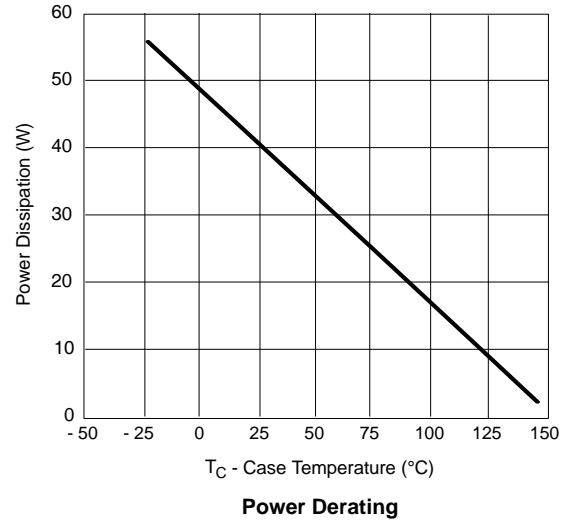
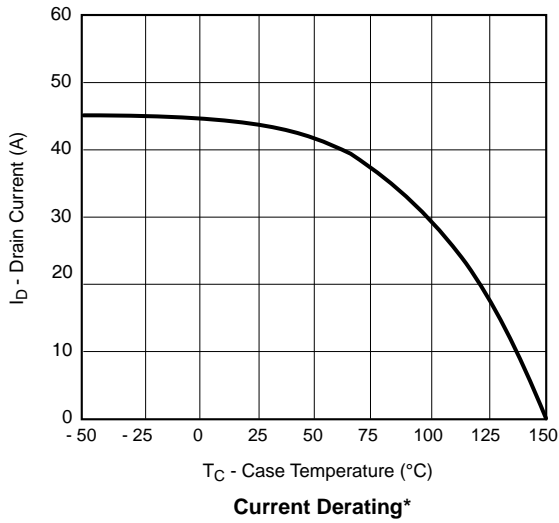


Threshold Voltage

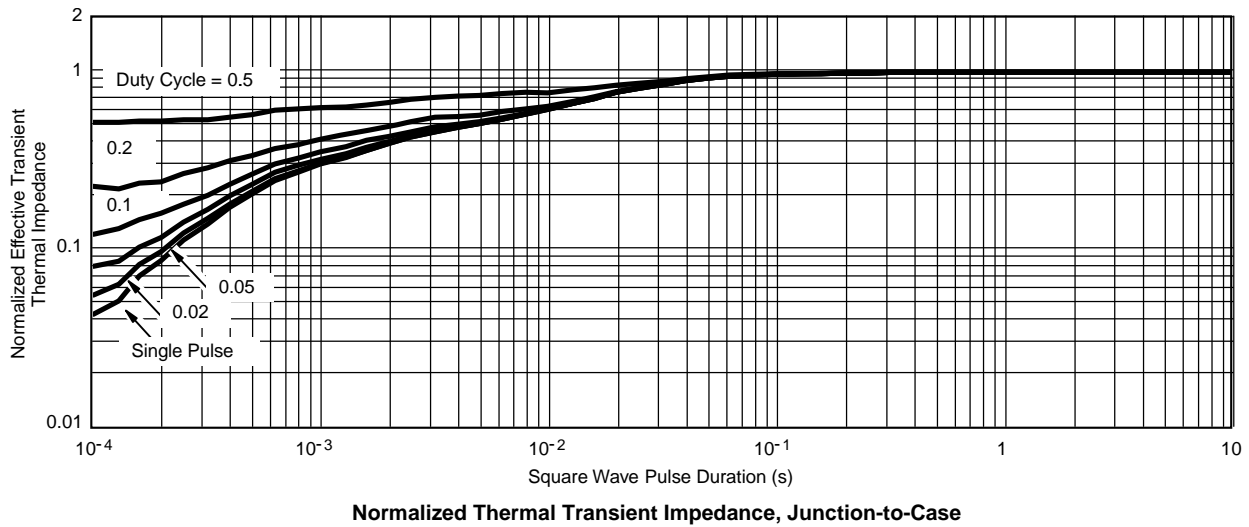


Safe Operating Area, Junction-to-Ambient
*V_{GS} > minimum V_{GS} at which r_{DS(on)} is specified

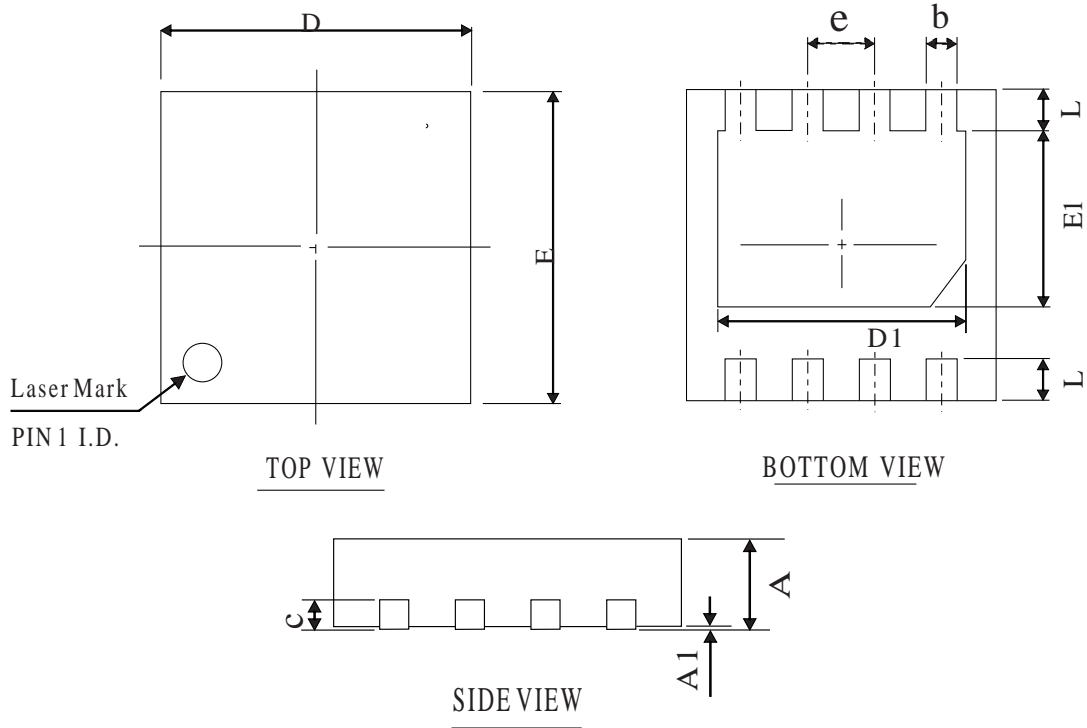
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



DFN3*3-8L PACKAGE OUTLINE



COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	0.60	0.75	0.90
A1	0.00	0.02	0.08
b	0.20	0.30	0.45
D	2.85	3.00	3.15
E	2.85	3.00	3.15
D1	2.10	2.40	2.70
E1	1.50	1.70	2.00
L	0.20	0.40	0.60
c	0.203 REF		
e	0.65 BSC		

OTHER DIMENSIONS

A	0.50	0.55	0.60
A	0.40	0.45	0.50

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