N-Channel 40 V (D-S) Power MOSFET

RoHS COMPLIANT

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (mΩ)(Typ.)	I_D (A)[a]	Q_g (Typ.)
40	0.68 at V_{GS} = 10 V	418	98 nC

FEATURES

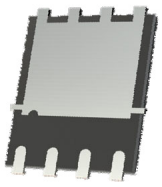
- DT-SGT Power MOSFET
- 100 % Rg and UIS tested
- High Power and Current Handing Capability
- AEC-Q101 Qualified for Automotive Applications

APPLICATIONS

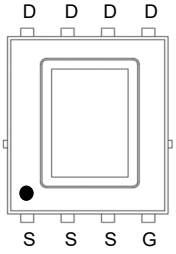
- POL Applications
- Ideal for High-Frequency Switching and Synchronous Ectification

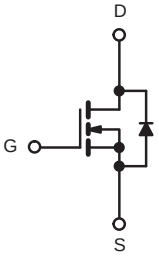
DFN5X6DSC-8L Pin Configuration

Top View



Bottom View





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)[a]	T_C = 25 °C	I_D	418	A
	T_C = 100 °C		295	
Pulsed Drain Current[b]		I_{DM}	1672	
Single Avalanche Energy		E_{AS}	1300	mJ
Maximum Power Dissipation[c]	T_C = 25 °C	P_D	231	W
	T_C = 100 °C		115	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction-to-Ambient (PCB Mount)[d]	R_{thJA}	50	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.65	

Notes

a. Calculated continuous current based on maximum allowablejunction temperature.
b. Repetitive rating; pulse width limited by max. junction temperature.
c. Pd is based on max. junction temperature, using junction-case thermal resistance.
d. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper,in a still air environment with Ta=25 °C.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2	-	4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	± 100	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 32 V, V_{GS} = 0 V, T_J = 125 °C	-	-	100	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ 5 V, V_{GS} = 10 V	418	-	-	A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A	-	0.68	0.82	mΩ
Forward Transconductance[a]	g_{fs}	V_{DS} = 5 V, I_D = 20 A	-	69	-	S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz	-	7589	-	pF
Output Capacitance	C_{oss}		-	4005	-	
Reverse Transfer Capacitance	C_{rss}		-	125	-	
Total Gate Charge[c]	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 20 A	-	98	-	nC
Gate-Source Charge[c]	Q_{gs}		-	29	-	
Gate-Drain Charge[c]	Q_{gd}		-	17.3	-	
Gate Resistance	R_g	f = 1 MHz	-	1.9	-	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 20 V, I_D=20A, R_{GEN} = 3 Ω V_{GS} = 10 V	-	9.5	-	ns
Rise Time[c]	t_r		-	21	-	
Turn-Off Delay Time[c]	$t_{d(off)}$		-	60	-	
Fall Time[c]	t_f		-	26	-	
Drain-Source Body Diode Ratings and Characteristics[b] (T_J = 25 °C)						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	-	-	418	A
Pulsed Current	I_{SM}		-	-	1672	A
Forward Voltage[a]	V_{SD}	I_F = 2 A, V_{GS} = 0 V	-	0.7	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 20 A, di/dt = 100 A/µs	-	75	-	ns
Reverse Recovery Charge	Q_{rr}		-	140	-	nC

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARAC TERISTICS (25 °C, unless otherwise noted)

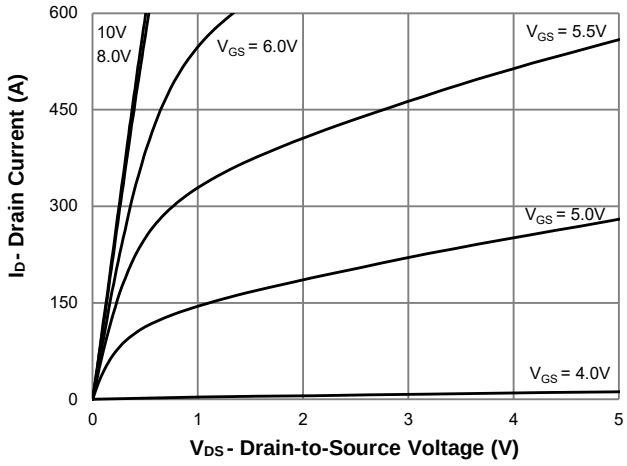


Figure 1: Output Characteristics

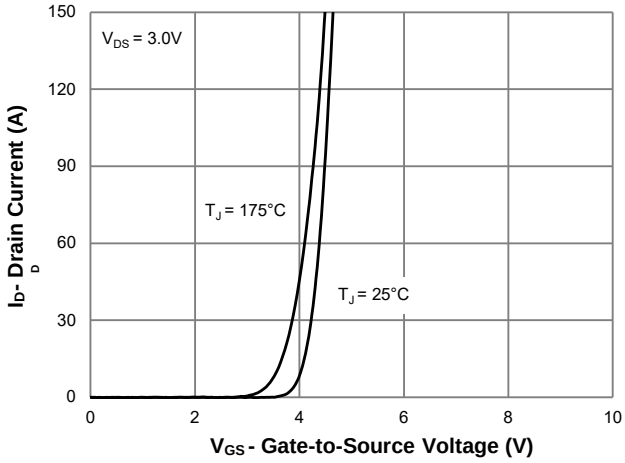


Figure 2: Transfer Characteristics

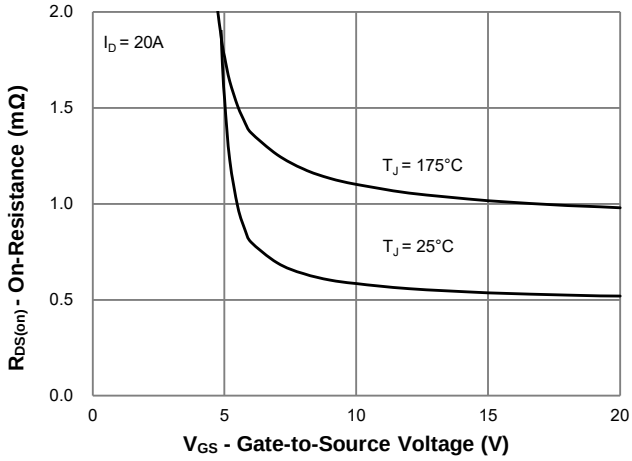


Figure 3: On-Resistance vs. Gate-Source Voltage

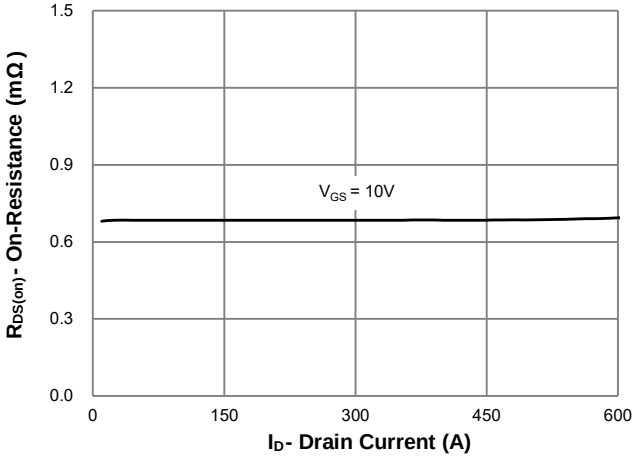


Figure 4: On-Resistance vs. Gate-Source Voltage

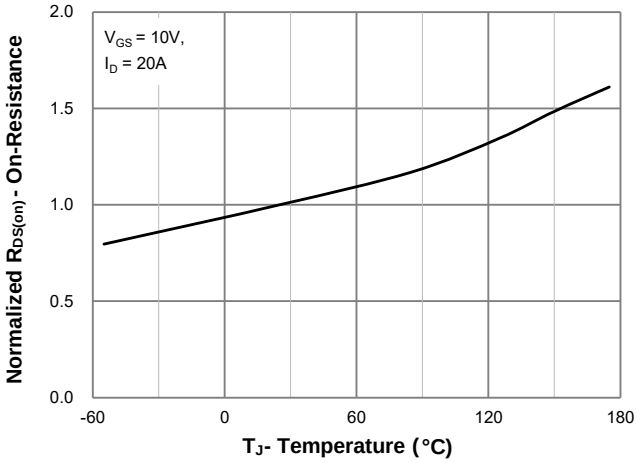


Figure 5: On-Resistance vs. Junction Temperature

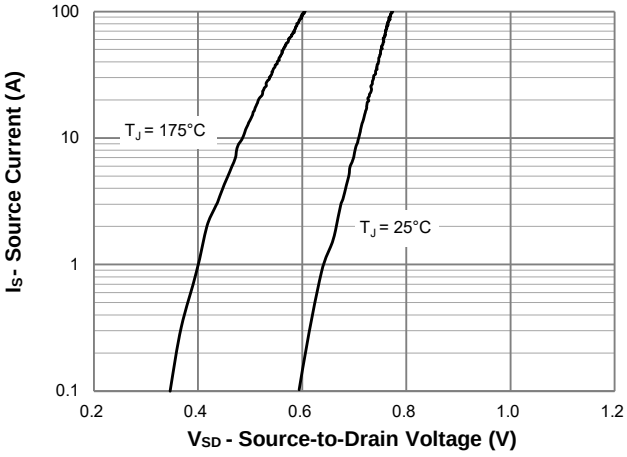


Figure 6: Source-Drain Diode Forward Voltage

TYPICAL CHARAC TERISTICS (25 °C, unless otherwise noted)

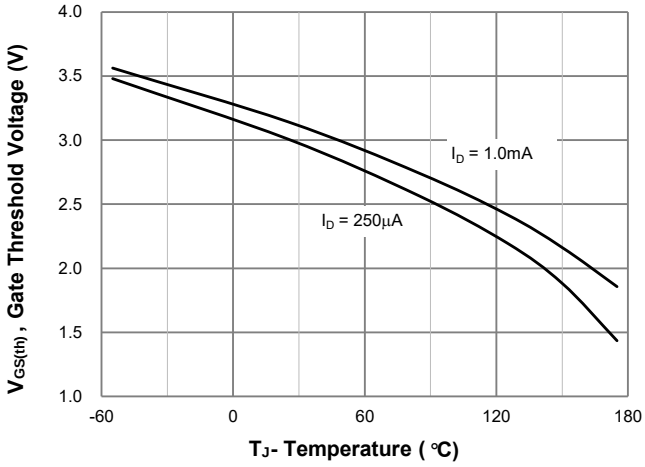


Figure 7: Gate Threshold Variation vs. Junction Temperature

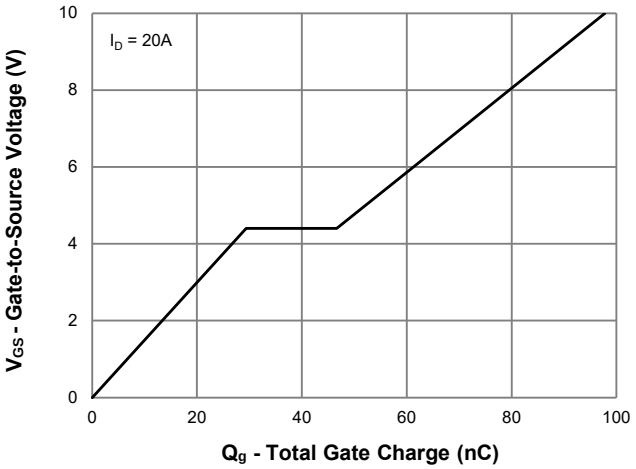


Figure 8: Gate Charge Characteristics

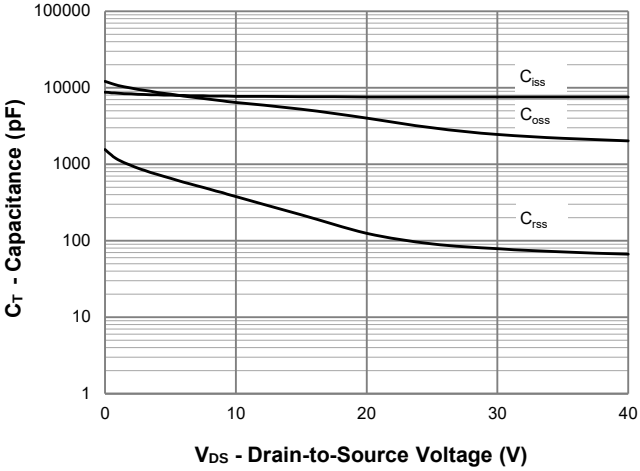


Figure 9: Capacitance Characteristics

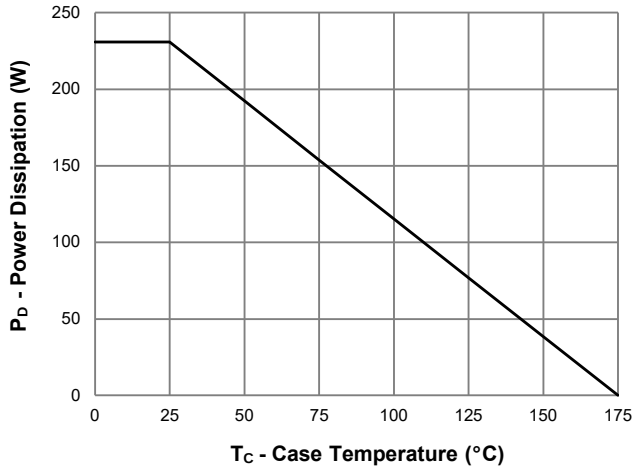


Figure 10: Power Derating

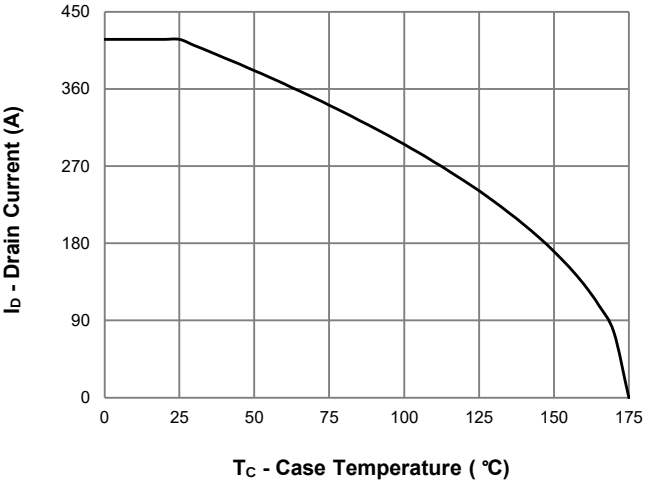


Figure 11: Current Derating

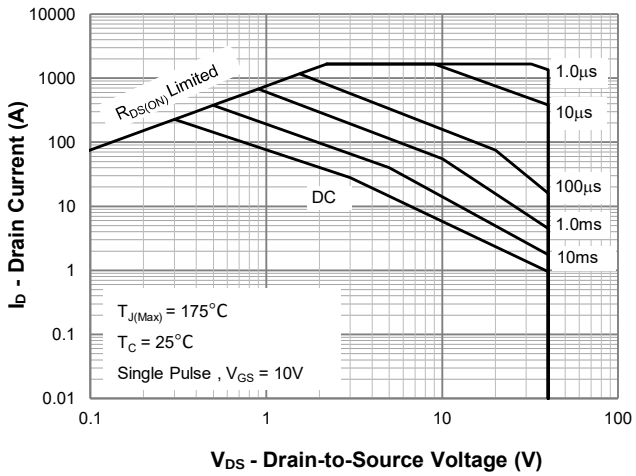


Figure 12: Safe Operating Area

TYPICAL CHARAC TERISTICS (25 °C, unless otherwise noted)

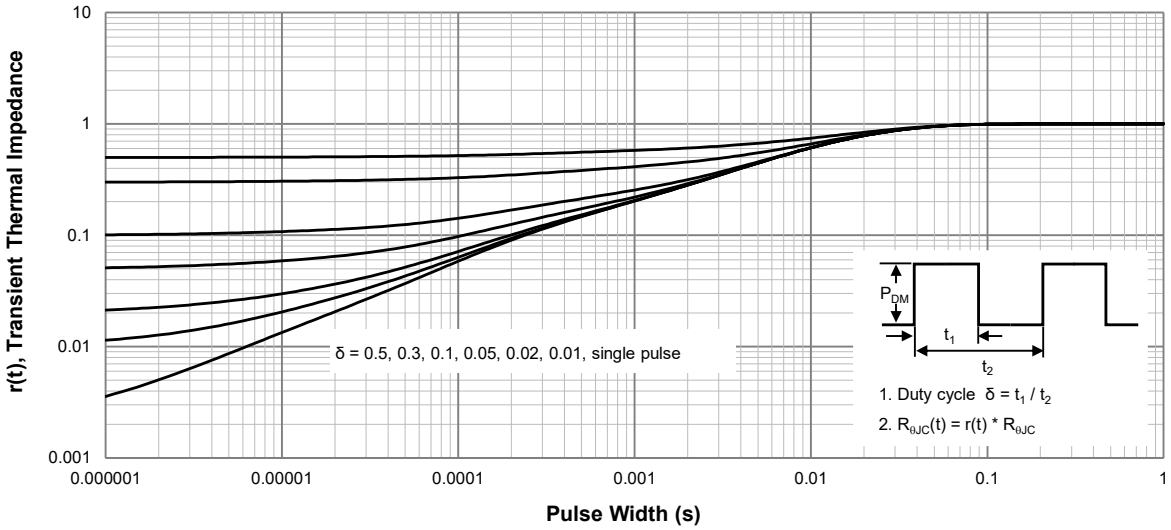
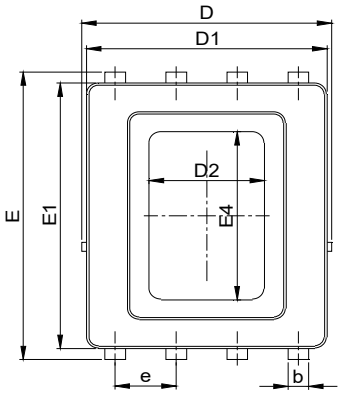
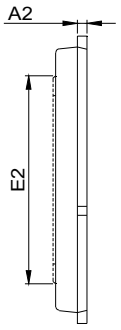


Figure 13: Normalized Maximum Transient Thermal Impedance

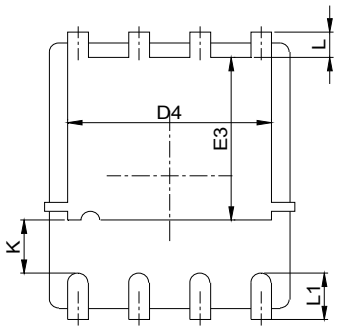
DFN5X6DSC-8L PACKAGE OUTLINE



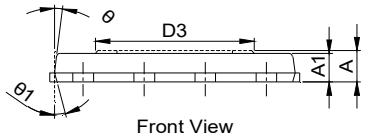
Top View



Side View



Bottom View



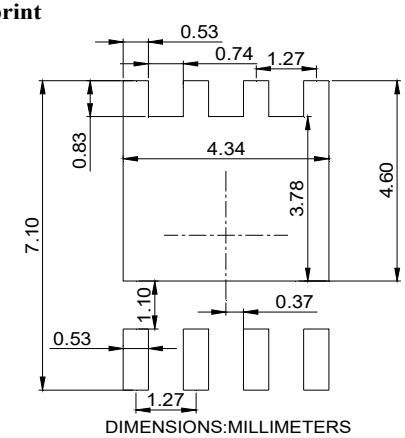
Front View

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
A1	0.60	---	0.75
A2	0.15	0.203	0.30
b	0.33	0.43	0.53
D	5.00	---	5.30
D1	5.00 Bsc		
D2	2.40 Bsc		
D3	2.80	3.30	3.80
D4	4.06	4.21	4.36
E	6.10	---	6.70
E1	6.00 Bsc		
E2	4.20	4.70	5.20
E3	3.525	3.675	3.825
E4	3.80 Bsc		
K	1.05	1.20	1.35
L	0.45	0.575	0.70
L1	0.925	1.05	1.175
θ	12° Bsc		
θ1	7° Bsc		

Recommended Soldering Footprint



DIMENSIONS:MILLIMETERS

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