N-Channel 40 V (D-S) Super Junction MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (mΩ)(Typ.)	I_D (A)[a]	Q_g (Typ.)
40	4 at V_{GS}= 10 V	80	17 nC
	5.2 at V_{GS} = 4.5 V		

FEATURES

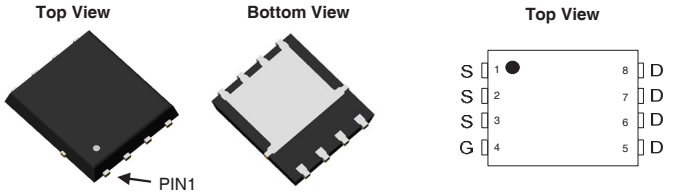
- DT-SJ Power MOSFET
- 100 % R_g and UIS tested
- Extremely Low $R_{DS(ON)}$

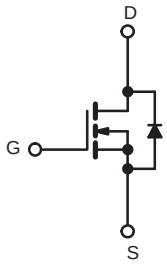
RoHS COMPLIANT

APPLICATIONS

- Synchronous Rectification
- Motor Drives and Uninterruptible Power Supplies

DFN5X6-8L Pin Configuration





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	80	A
	T_C = 100 °C		54	
Pulsed Drain Current		I_{DM}	320	
Single Avalanche Energy [a]	L = 0.5 mH	E_{AS}	275	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	60[b,c]	W
	T_C = 100 °C		30[b,c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	°C
Soldering Recommendations (Peak Temperature)			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient (PCB Mount)[b,d]	t ≤ 10 s	R_{thJA}	24.6	°C/W
Junction-to-Case (Drain)	Steady State	R_{thJC}	2.5	

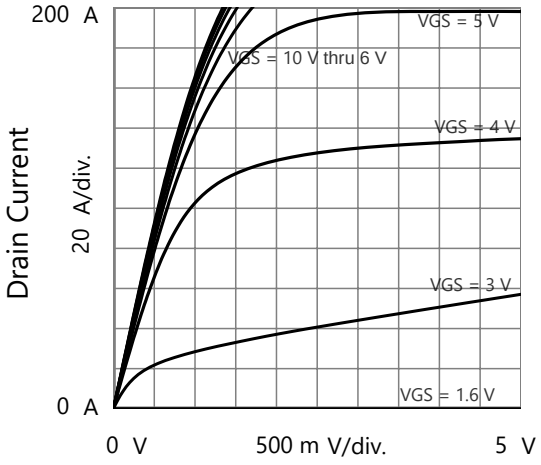
Notes:
a. T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under steady state conditions is 40 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA	40			V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	µA
		V_{DS} = 32 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	80			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		4	4.8	mΩ
		V_{GS} = 4.5 V, I_D = 20 A		5.2	6.5	
Forward Transconductance[a]	g_{fs}	V_{DS} = 4.5 V, I_D = 20 A		75		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		1030		pF
Output Capacitance	C_{oss}			580		
Reverse Transfer Capacitance	C_{rss}			20		
Total Gate Charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 20 A		17		nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2.6		
Gate Resistance	R_g	f = 1 MHz		2.5		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 1Ω I_D ≅ 20 A, V_{GEN} = 10 V, R_g = 3 Ω		22		ns
Rise Time	t_r			15		
Turn-Off DelayTime	$t_{d(off)}$			45		
Fall Time	t_f			18		
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I_S	T_C = 25 °C			80	A
Pulse Diode Forward Current (100 µs)	I_{SM}				320	
Body Diode Voltage	V_{SD}	I_S = 1 A			1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20 A, dI/dt = 100 A/µs, T_J = 25 °C		25		ns
Body Diode Reverse Recovery Charge	Q_{rr}			58		nC

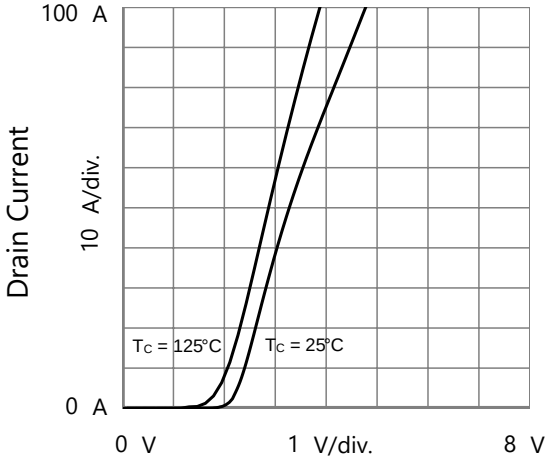
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

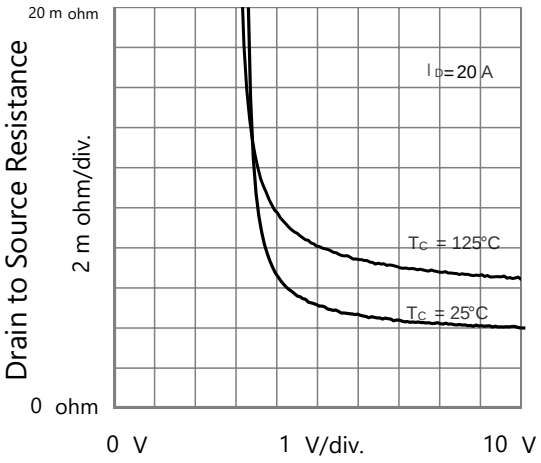
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



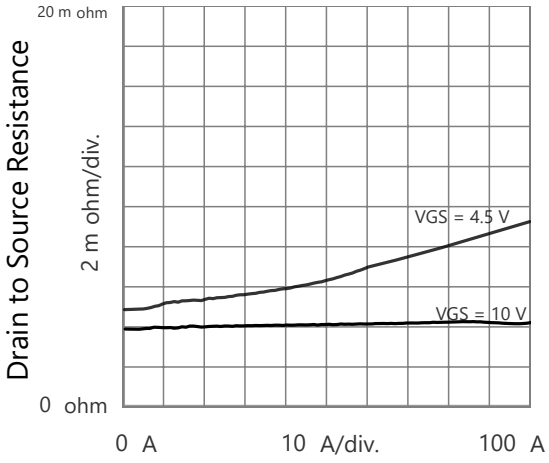
Drain to Source Voltage
Output Characteristics



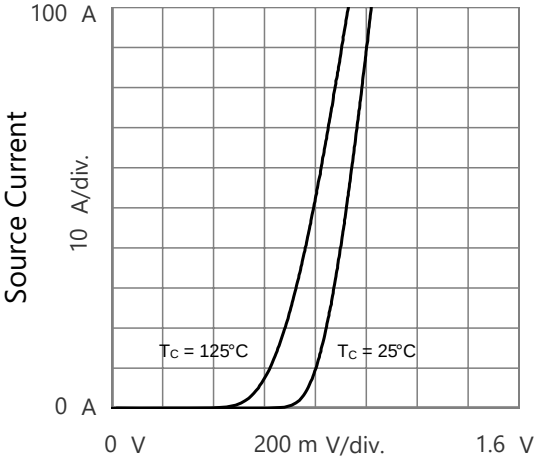
Gate to Source Voltage
Transfer Characteristics



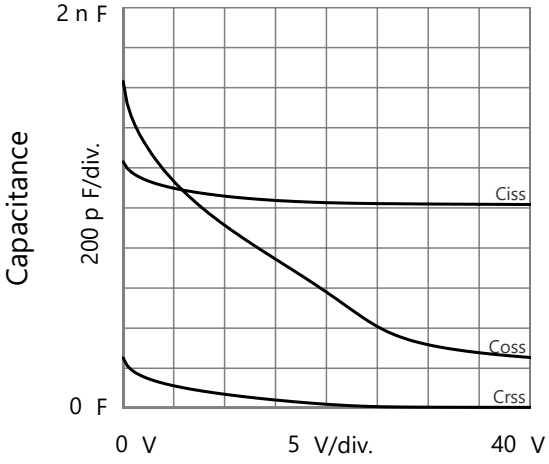
Gate to Source Voltage
Drain to Source Resistance vs. Gate to Source Voltage



Drain Current
Drain to Source Resistance vs. Drain Current

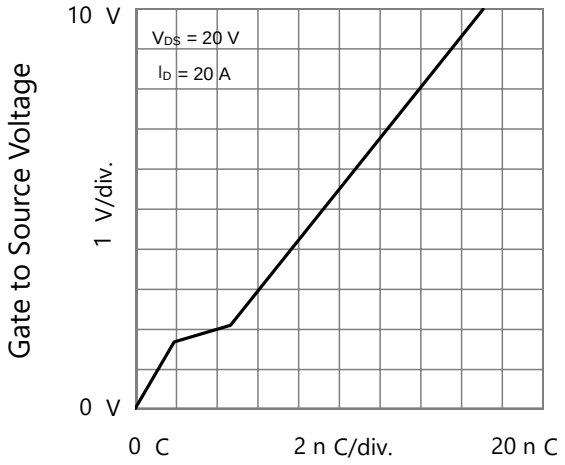


Source to Drain Voltage
Body Diode Forward Characteristics

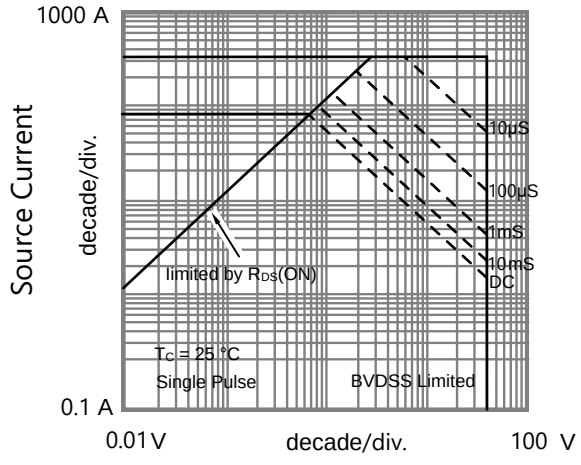


Drain to Source Voltage
Capacitances

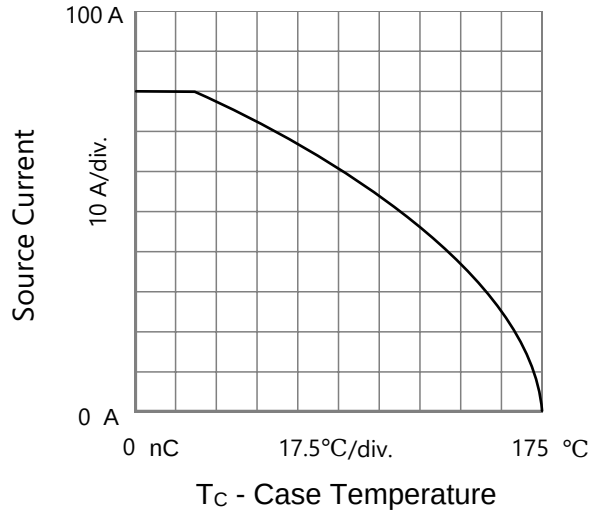
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

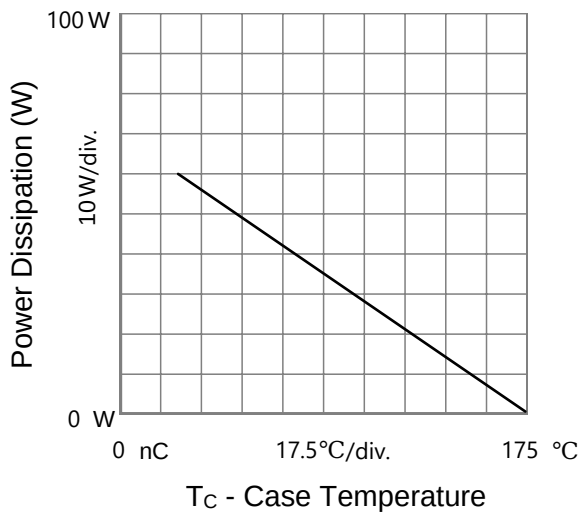


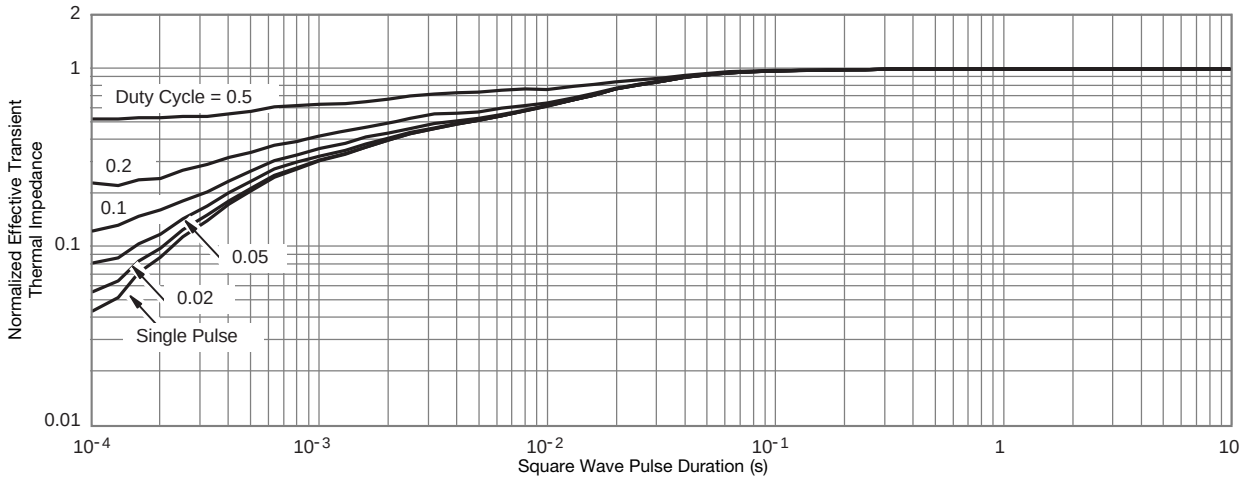
Gate to Source Voltage vs. GateCharge



Safe Operating Area, Junction-to-Ambient







Normalized Thermal Transient Impedance, Junction-to-Case

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