



Dual N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}$ (Ω)	I _D (A) ^d	Q _g (Typ.)			
100	0.017 at V _{GS} = 10 V	30	16 nC			

FEATURES

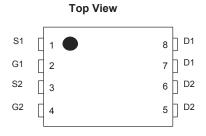
- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested

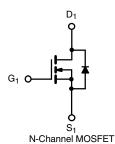


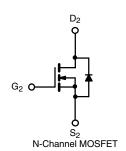
RoHS

APPLICATIONS

- · Synchronous Buck Shoot-Through Resistant
- Optimized for Primary Side Switch







ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V_{DS}	100	V		
Gate-Source Voltage	V _{GS}	± 20	7 v			
Continuous Drain Current (T _{.I} = 150 °C) ^a	T _A = 25 °C	l _s	30			
Continuous Drain Current (1) = 150 °C)	T _A = 70 °C	I _D	19			
Pulsed Drain Current		I _{DM}	120	Α		
Continuous Source Current (Diode Conduction) ^a	I _S	30				
Single Avalanche Current L = 0.1 mH		I _{AS}			27	
Single Avalanche Energy		E _{AS}	68	mJ		
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	49	w		
Maximum Power Dissipation	T _A = 70 °C	υ, υ	33	7		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C		
Soldering Recommendations (Peak Temperature)		260				

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	56	85	°C/W
Maximum Junction-to-Ambient	Steady State		80	110	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.1	3.0	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.



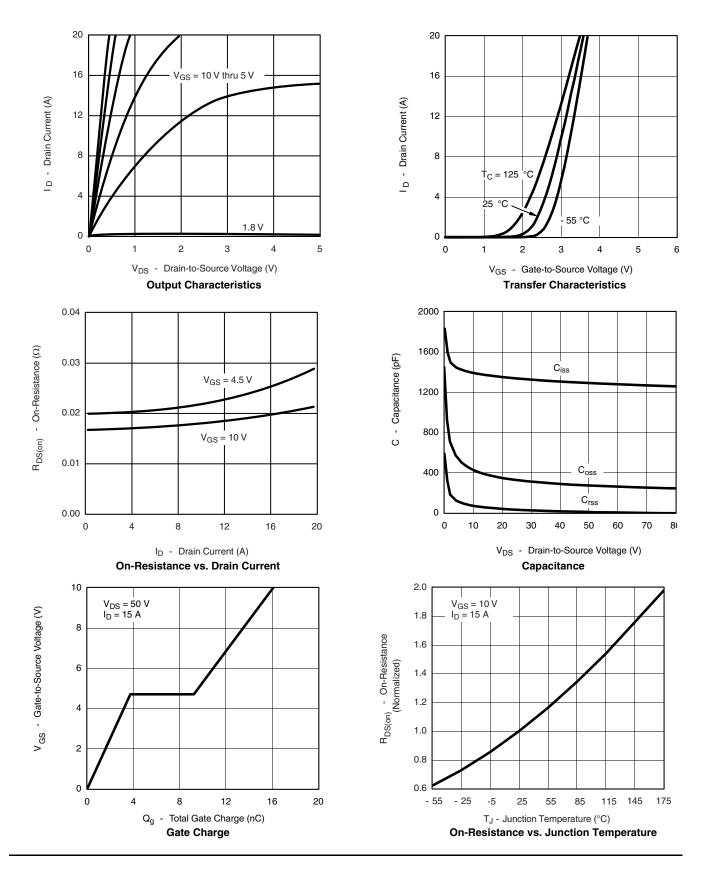
Parameter	Symbol	ool Test Conditions		Тур.	Max.	Unit	
Static			·				
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$			3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtaga Dvain Current		V _{DS} = 80 V, V _{GS} = 0 V			1	μΑ	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
	В	V _{GS} = 10 V, I _D = 15 A		0.017	0.022	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 10 A		0.020	0.028	Ω	
Forward Transconductance ^a	g_{fs} $V_{DS} = 15 \text{ V}, I_D = 10 \text{ A}$		18		S		
Diode Forward Voltage ^a	de Forward Voltage ^a V _{SD} I _S = 2.9 A, V _{GS} = 0 V			0.8	1.2	V	
Dynamic ^b	·						
Input Capacitance	C _{iss}			1345			
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		306		pF	
Reverse Transfer Capacitance	C _{rss}			13		7	
Total Gate Charge	Q_g			16	24		
Gate-Source Charge	Q_{gs} $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$			3.8		nC	
Gate-Drain Charge	Q_{gd}			5.5			
Gate Resistance	R_g			2.2		Ω	
Turn-On Delay Time	t _{d(on)}			5			
Rise Time	t_r $V_{DD} = 50 \text{ V}, R_L = 50 \Omega$			3			
Turn-Off Delay Time	t _{d(off)}	$t_{d(off)}$ $I_D \cong 1 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 6 \Omega$		20		ns	
Fall Time	t _f			5		113	
Source-Drain Reverse Recovery Time		I _F = 2.9 A, dI/dt = 100 A/μs		50			

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing.

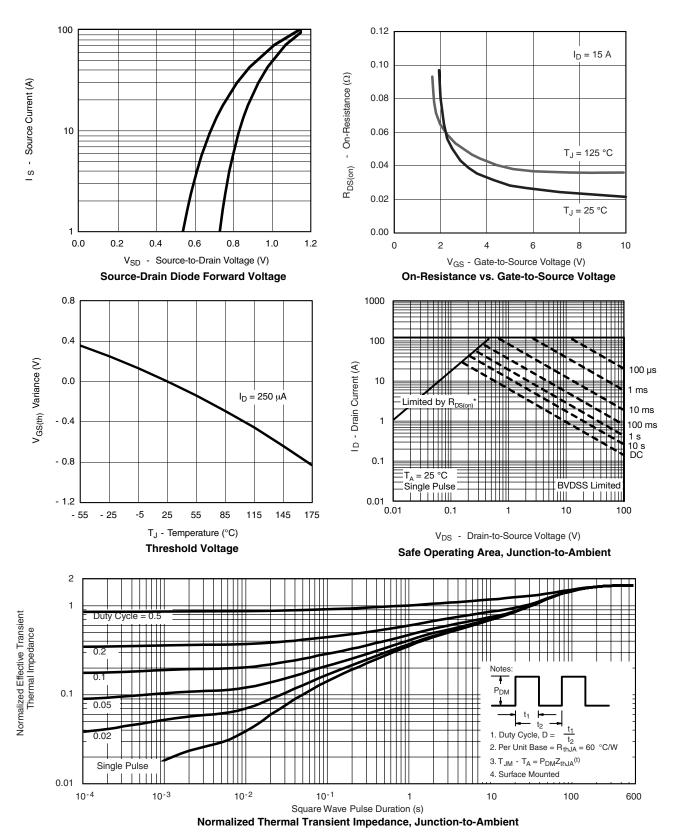


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



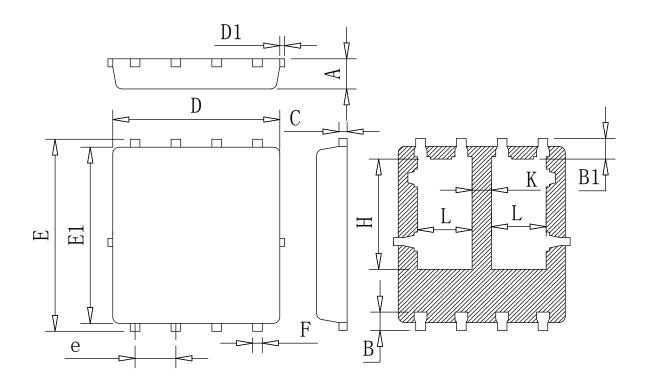


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DTQ6D002 www.din-tek.jp

DFN5X6-8L-D PACKAGE OUTLINE



COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)

Symbol	Min	Тур	Max
A	0.85	0.95	1.05
В	0.46	0.58	0.73
B1	0.52	0.65	0.78
С	0.18	0.254	0.32
D	4.70	5.20	5.50
D1	-	-	0.18
Е	5.75	6.05	6.35
E1	5.35	5.65	5.85
e	1.15	1.27	1.50
F	0.15	0.30	0.50
Н	3.15	3.47	3.80
L	1.35	1.70	2.10
K	0.35	0.60	1.00





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