Dual N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (mΩ)(Typ.)	I_D (A)[d]	Q_g (Typ.)
100	56 at V_{GS} = 10 V	15	20 nC

FEATURES

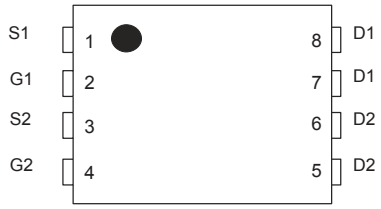
- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested

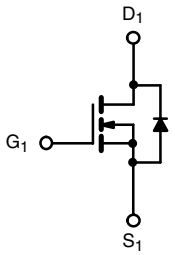
Pb-free
RoHS COMPLIANT

APPLICATIONS

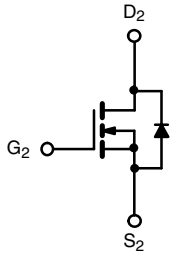
- Synchronous Buck Shoot-Through Resistant
- Optimized for Primary Side Switch

Top View





N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	15	A
	T_A = 70 °C		9	
Pulsed Drain Current		I_{DM}	35	
Continuous Source Current (Diode Conduction)[a]		I_S	15	
Single Avalanche Current	L = 0.1 mH	I_{AS}	13	
Single Avalanche Energy		E_{AS}	8	mJ
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	33	W
	T_A = 70 °C		2.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C
Soldering Recommendations (Peak Temperature)			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	15	25	°C/W
	Steady State		40	50	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4	5	

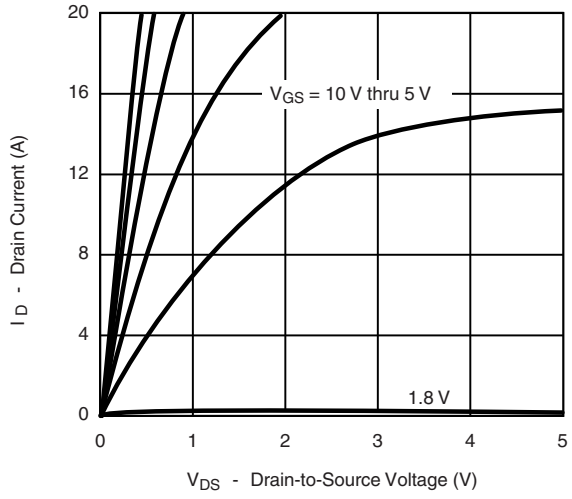
Notes:
a. Surface Mounted on 1" x 1" FR4 board.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55 °C			5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A		56	68	mΩ
		V_{GS} = 4.5 V, I_D = 3 A		75	96	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 5 A		18		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1 A, V_{GS} = 0 V		0.7	1	V
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		1245		pF
Output Capacitance	C_{oss}			106		
Reverse Transfer Capacitance	C_{rss}			63		
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 5 A		20		nC
Gate-Source Charge	Q_{gs}			3.8		
Gate-Drain Charge	Q_{gd}			5.5		
Gate Resistance	R_g			5		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 50 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 6 Ω		5		ns
Rise Time	t_r			3		
Turn-Off Delay Time	$t_{d(off)}$			20		
Fall Time	t_f			5		
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 5 A, dI/dt = 100 A/µs		50		

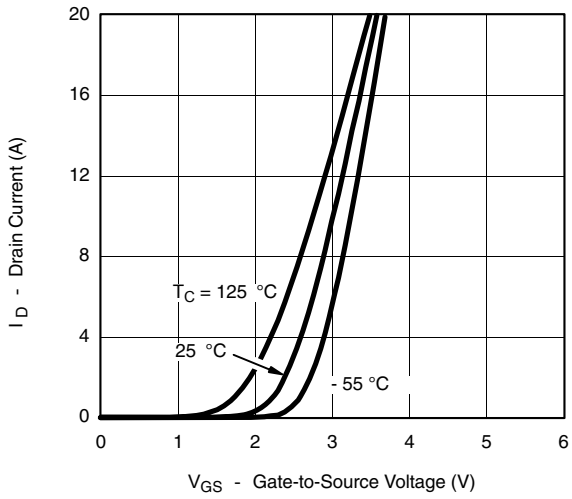
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

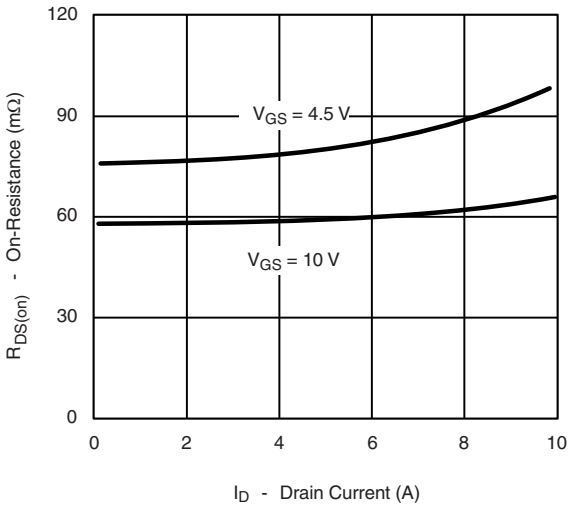
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



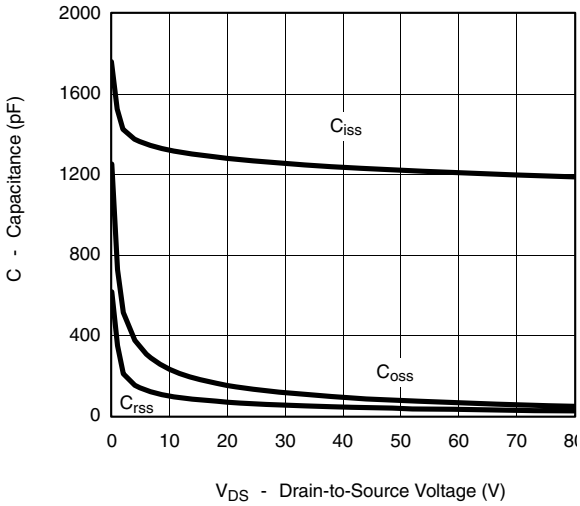
Output Characteristics



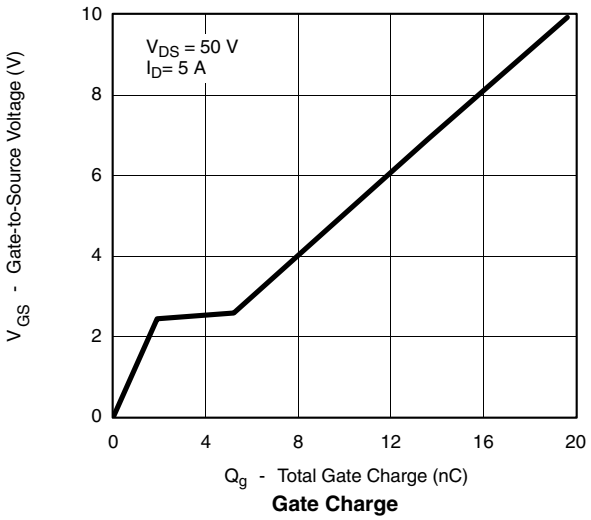
Transfer Characteristics



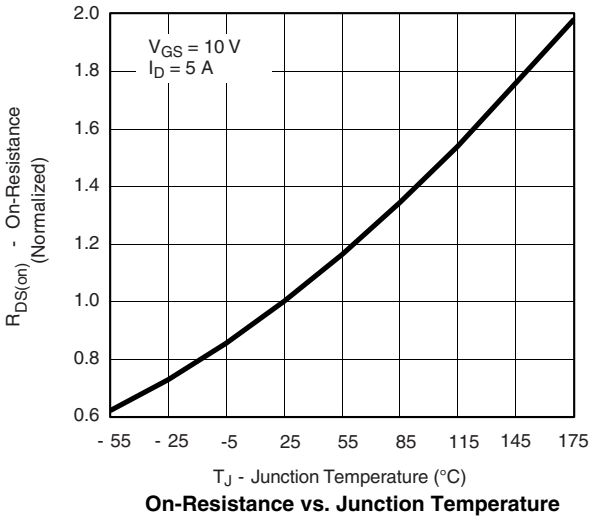
On-Resistance vs. Drain Current



Capacitance

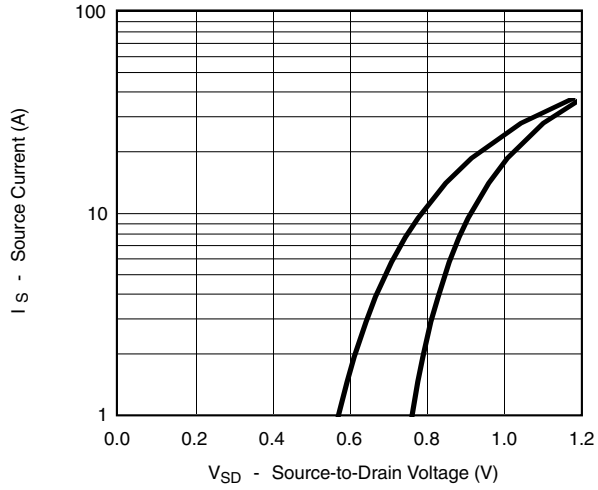


Gate Charge

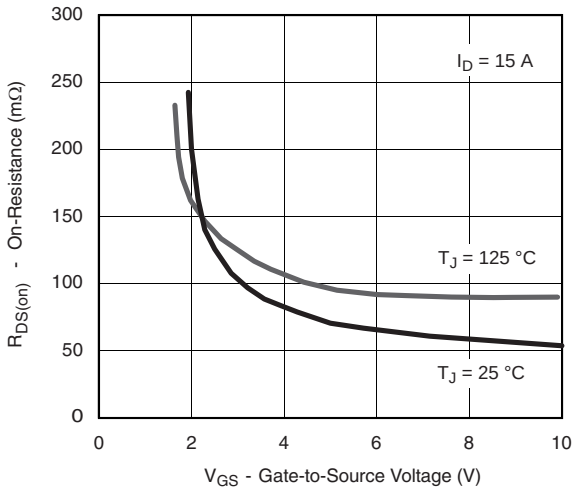


On-Resistance vs. Junction Temperature

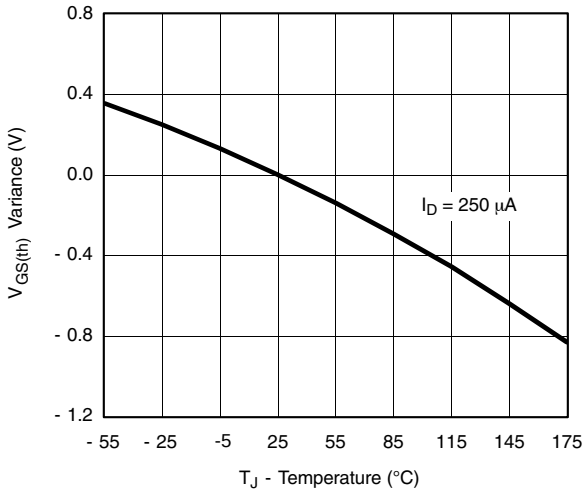
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



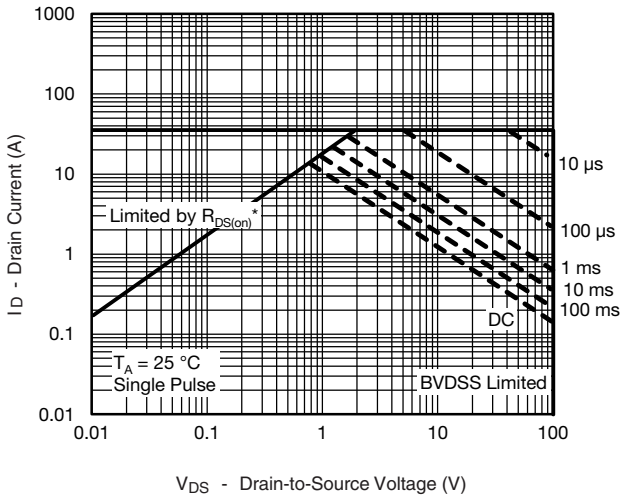
Source-Drain Diode Forward Voltage



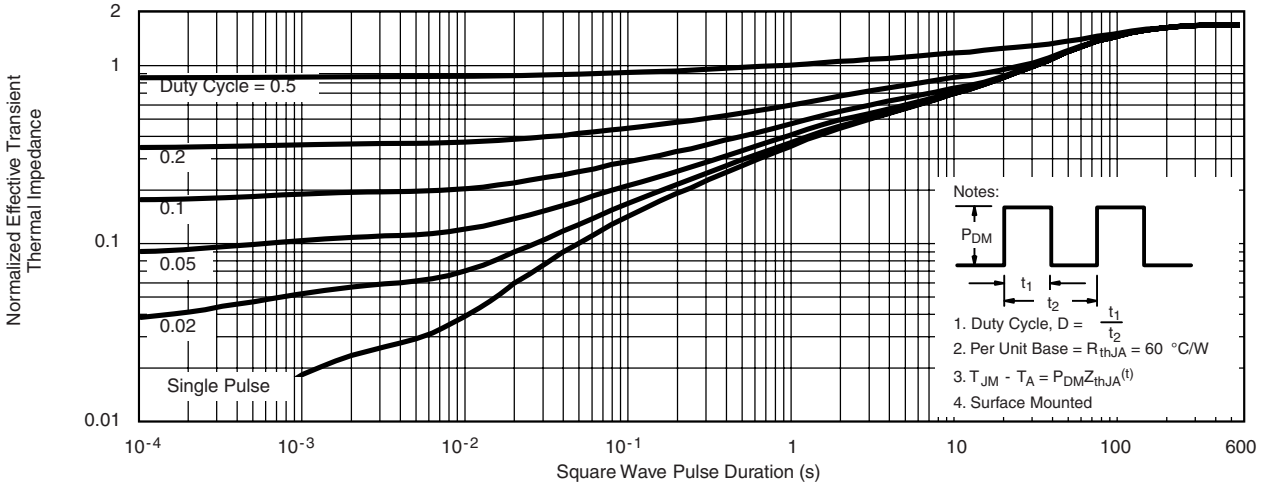
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

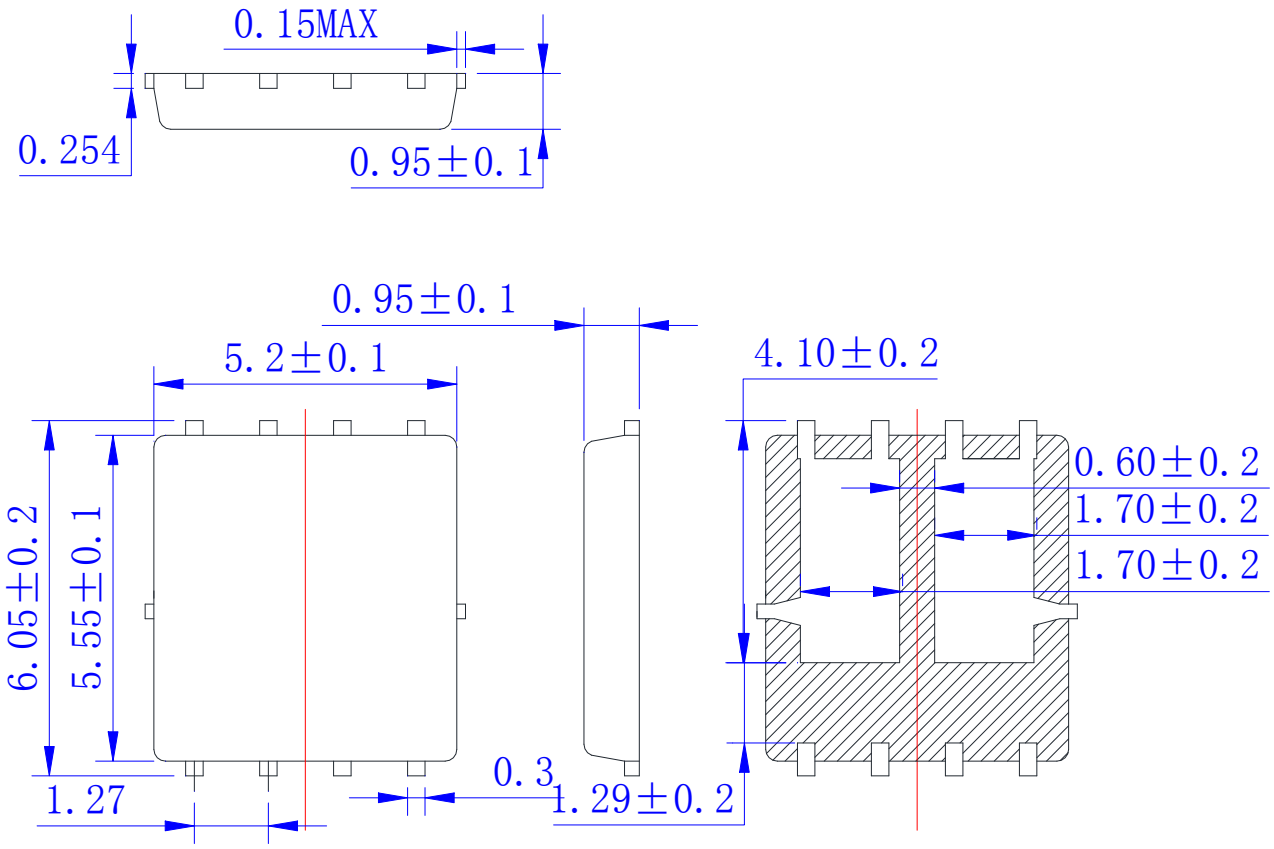


Safe Operating Area, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

DFN5*6-8L Package Outline



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