

RoHS

COMPLIANT

N-Channel 650 V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (mΩ)(Typ.)	I _D (A)	Q _g (Typ.)		
650	180 at V _{GS} = 10 V	20	25 nC		

DFN8X8 Pin Configuration

Bottom View

Top View

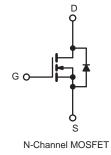
GS

D

Extre

· Excellent stability and uniformity

APPLICATIONS



ABSOLUTE MAXIMUM RATINGS ($T_C = 25 \text{ °C}$, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	650	V		
Gate-Source Voltage	V _{GS}	± 30	7 V		
Continuous Drain Current (T _J = 150 °C) ^a	T _C = 25 °C	1-	20		
	T _C = 100 °C	I _D	12.5	А	
Pulsed Drain Current ^b		I _{DM}	60		
Single Avalanche Energy		E _{AS}	230	mJ	
Meyimum Dewer Dissinction	T _C = 25 °C	P	151	w	
Maximum Power Dissipation ^c	T _C = 100 °C		60.4	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction-to-Ambient (PCB Mount) ^d	ent (PCB Mount) ^d R _{thJA} 62				
Junction-to-Case (Drain)	R _{thJC}	0.82	°C/W		

Notes

a. Calculated continuous current based on maximum allowablejunction temperature.

- b. Repetitive rating; pulse width limited by max. junction temperature.
- c. Pd is based on max. junction temperature, using junction-case thermal resistance.
- d. The value of ReuA is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with Ta=25 °C.

• DT-SJ Power MOSFET

- Low RDS(ON)×FOM
- emely low switching loss

PC power

FEATURES

- LED lighting
- Server power



DTQ820N065SJ

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static					·	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS}=0~V,~I_D=250~\mu A$	650	-	-	V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS},\ I_D=250\ \mu A$	2.9	-	3.9	v
Gate-Body Leakage	I _{GSS}	$V_{DS}=0~V,~V_{GS}=\pm~30~V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 650 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	μA
Drain-Source On-State Resistance a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	-	180	200	mΩ
Drain-Source On-State Resistance -	US(on)	V_{GS} = 10 V, I_{D} = 10 A, T_{j} = 150 $^{\circ}\mathrm{C}$	-	433	-	
Dynamic ^b						
Input Capacitance	C _{iss}		-	1485	-	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 50 \text{ V}, f = 100 \text{ kHz}$	-	101	-	pF
Reverse Transfer Capacitance	C _{rss}		-	5	-	1
Total Gate Charge ^c	Qg		-	25	-	
Gate-Source Charge ^c	Q _{gs}	V_{DS} = 400 V, V_{GS} = 10 V, I_{D} = 10 A	-	7.1	-	nC
Gate-Drain Charge ^c	Q _{gd}		-	7	-	
Gate Resistance	R _g	f = 1 MHz	-	5	-	Ω
Turn-On Delay Time ^c	t _{d(on)}		-	14	-	
Rise Time ^c	t _r	$V_{DS} = 400 \text{ V}, I_D = 10 \text{ A},$	-	10	-	
Turn-Off Delay Time ^c	t _{d(off)}	$V_{GS} = 10 V, R_g = 2\Omega$	-	30	-	ns
Fall Time ^c	t _f		-	2	-	
Drain-Source Body Diode Ratings a	nd Characteris	stics ^b (T _C = 25 °C)				-
Continuous Source Current	۱ _S	T _C = 25 °C	-	-	20	А
Pulsed Current	I _{SM}		-	-	60	А
Forward Voltage ^a	V _{SD}	$I_{S} = 10 \text{ A}, V_{GS} = 0 \text{ V}$	-	-	1.1	V
Reverse Recovery Time	t _{rr}		-	370	-	ns
Reverse Recovery Charge	Q _{rr}	$I_S = 10$ A, di/dt = 100 A/ μ s	-	6.2	-	μC
Peak reverse recovery current	I _{rrm}		-	30.9	-	А

Notes

a. Pulse test; pulse width $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%.$

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

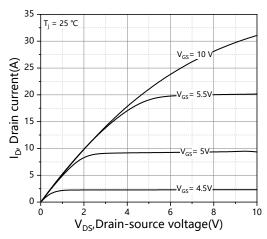


Figure 1. Typ. output characteristics Tj=25°C

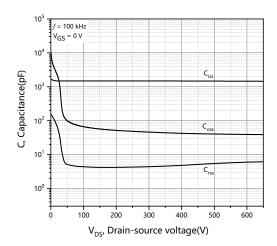


Figure 3. Typ. capacitances

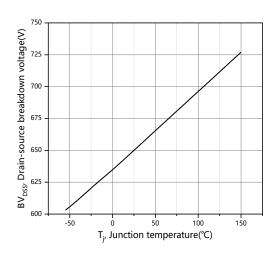


Figure 5. Drain-source breakdown voltage

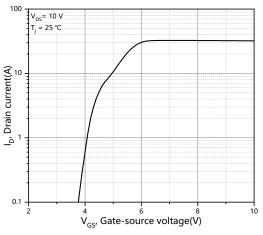


Figure 2. Typ. transfer characteristics

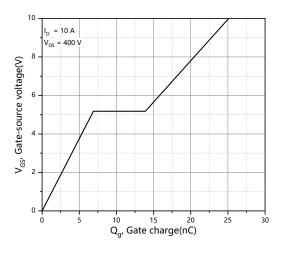


Figure 4. Typ. gate charge

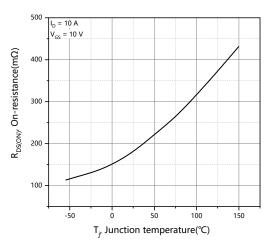
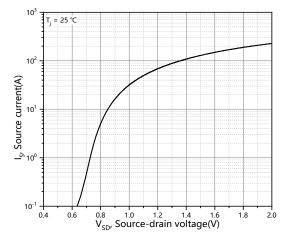
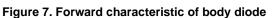


Figure 6. Drain-source on-state resistance



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





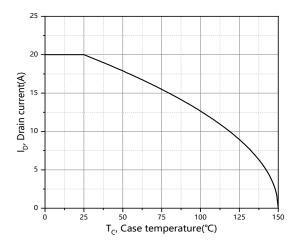


Figure 9. Drain current

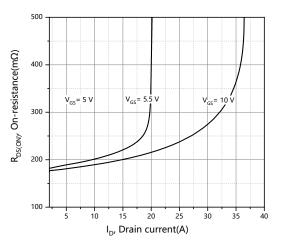


Figure 8. Drain-source on-state resistance

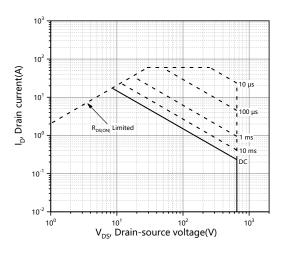


Figure 10. Safe operation area Tc=25°C

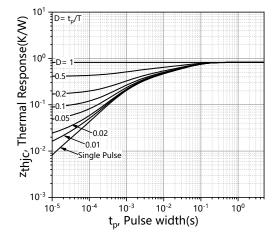
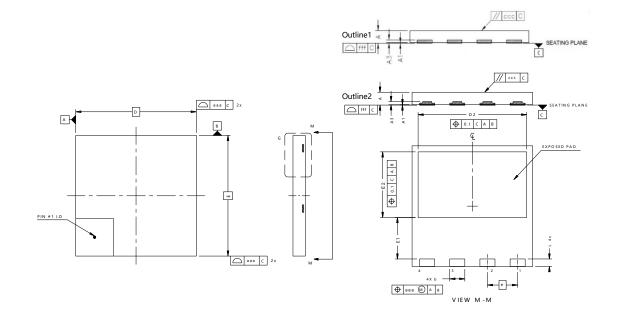


Figure 11. Max. transient thermal impedance



Package Information www.din-tek.jp

DFN8*8 PACKAGE OUTLINE



Symbol	mm			
	Min	Max		
А	0.75	1.15		
A1	0.00	0.05		
A3	0.10	0.30		
b	0.90	1.10		
D	7.85	8.15		
E	7.85	8.15		
D2	7.10	7.30		
E1	2.65	2.85		
E2	4.25	4.45		
е	2.0 BSC			
L	0.40	0.60		
aaa	0.1			
999	0.05			
ссс	0.05			
fff	0.05			



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