N-Channel 500V (D-S) Power MOSFET

RoHS COMPLIANT

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	500	
$R_{DS(on)}$ max. at 25 °C (Ω)	V_{GS} = 10 V	0.78
Q_g max. (nC)	50	
Q_{gs} (nC)	6	
Q_{gd} (nC)	10	
Configuration	Single	

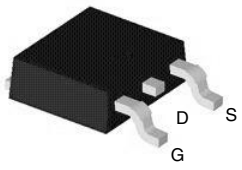
FEATURES

- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

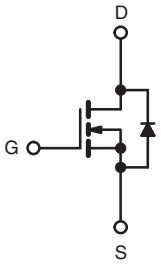
APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial

TO-252 Pin Configuration



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	10	A
		T_C = 100 °C		6.2	
Pulsed Drain Current [a]			I_{DM}	20	
Linear Derating Factor				0.91	W/°C
Single Pulse Avalanche Energy			E_{AS}	105	mJ
Maximum Power Dissipation			P_D	126	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	V_{DS} = 0 V to 80 % V_{DS}		dV/dt	70	V/ns
Reverse Diode dV/dt [c]				27	
Soldering Recommendations (Peak Temperature) [b]	for 10 s			300	°C

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	50	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.99	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. 1.6 mm from case.
c. $I_{SD} \leq I_D$, dI/dt = 100 A/µs, starting T_J = 25 °C.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.60	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 6 A	-	0.65	0.78	Ω
Forward Transconductance	g_{fs}	V_{DS} = 30 V, I_D = 6 A	-	6.8	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	1420	-	pF
Output Capacitance	C_{oss}		-	55	-	
Reverse Transfer Capacitance	C_{rss}		-	6	-	
Effective Output Capacitance, Energy Related [a]	$C_{o(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	45	-	
Effective Output Capacitance, Time Related [b]	$C_{o(tr)}$		-	131	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 6 A, V_{DS} = 400 V	-	25	50	nC
Gate-Source Charge	Q_{gs}		-	6	-	
Gate-Drain Charge	Q_{gd}		-	10	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 6 A, V_{GS} = 10 V, R_g = 9.1 Ω	-	13	-	ns
Rise Time	t_r		-	16	-	
Turn-Off Delay Time	$t_{d(off)}$		-	29	-	
Fall Time	t_f		-	12	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain	-	0.92	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	10	A
Pulsed Diode Forward Current	I_{SM}		-	-	20	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 7.5 A, V_{GS} = 0 V	-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 6 A, dI/dt = 100 A/µs, V_R = 25 V	-	144	-	ns
Reverse Recovery Charge	Q_{rr}		-	175	-	nC
Reverse Recovery Current	I_{RRM}		-	19	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

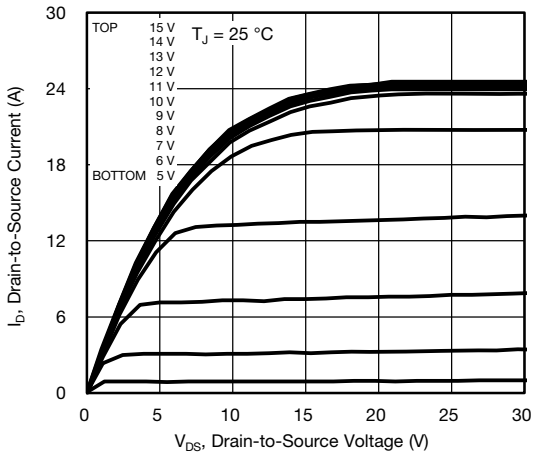


Fig. 1 - Typical Output Characteristics

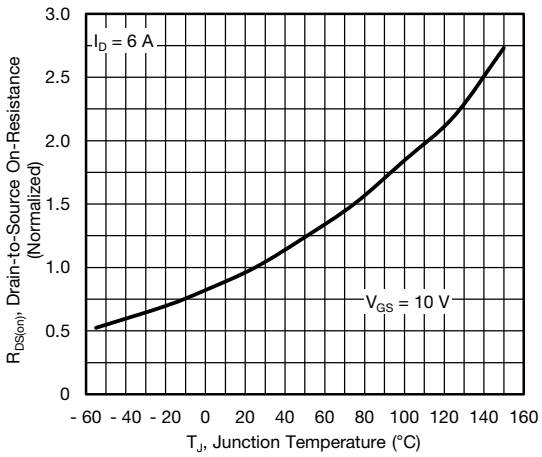


Fig. 4 - Normalized On-Resistance vs. Temperature

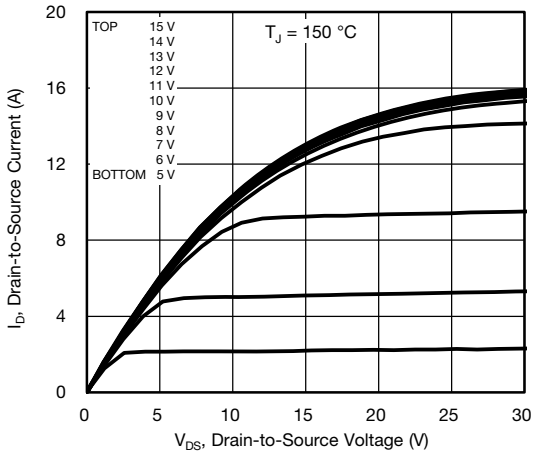


Fig. 2 - Typical Output Characteristics

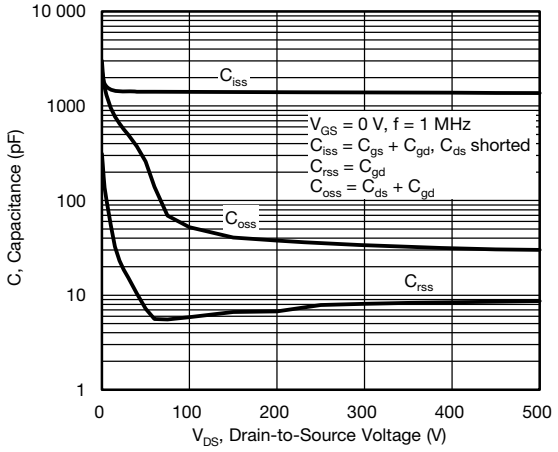


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

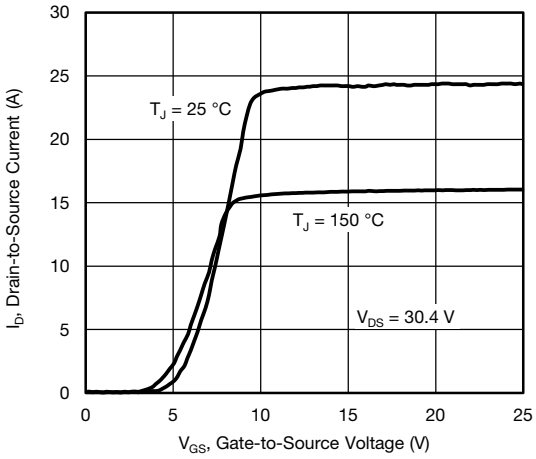


Fig. 3 - Typical Transfer Characteristics

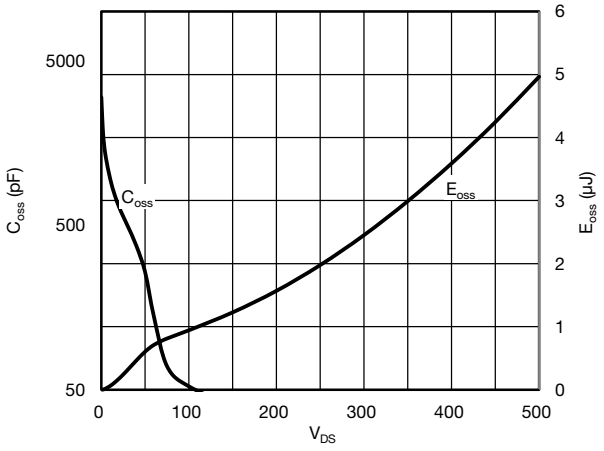


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

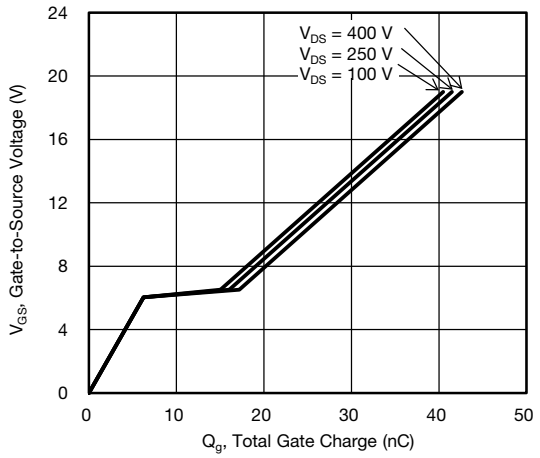


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

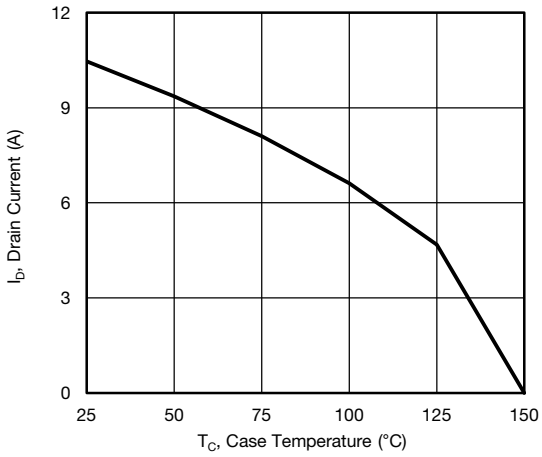


Fig. 10 - Maximum Drain Current vs. Case Temperature

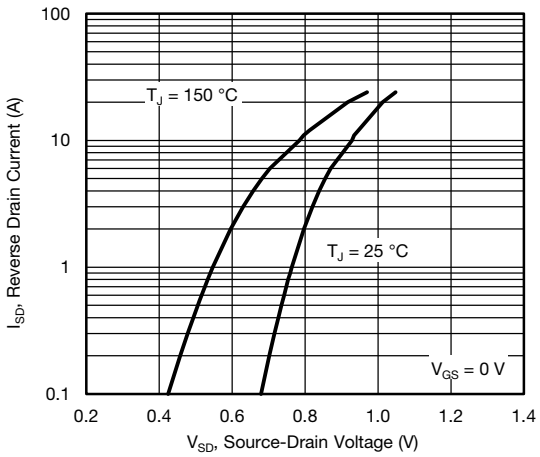


Fig. 8 - Typical Source-Drain Diode Forward Voltage

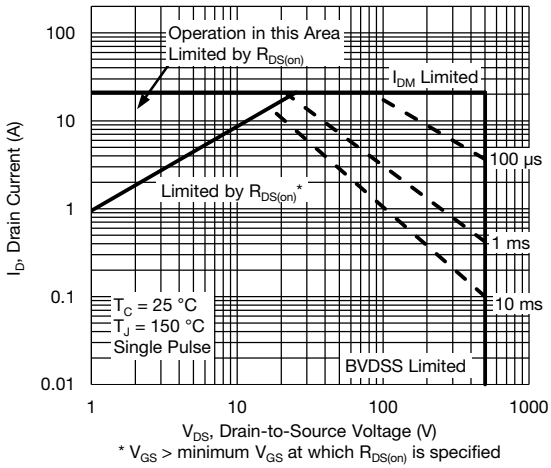


Fig. 9 - Maximum Safe Operating Area

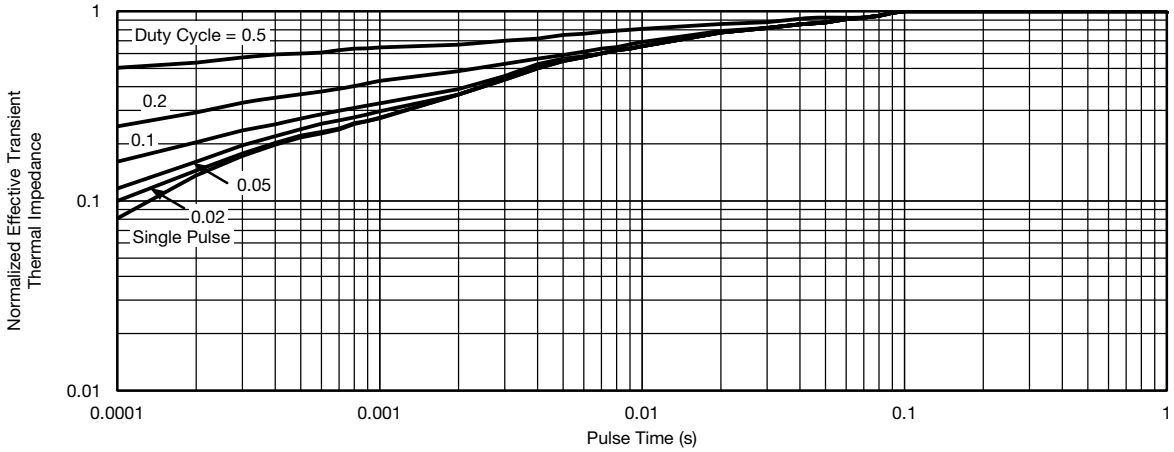


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

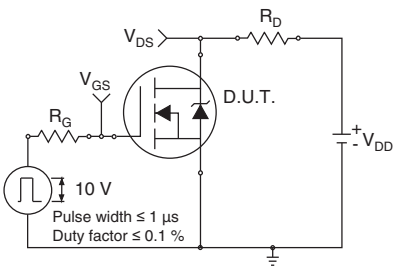


Fig. 12 - Switching Time Test Circuit

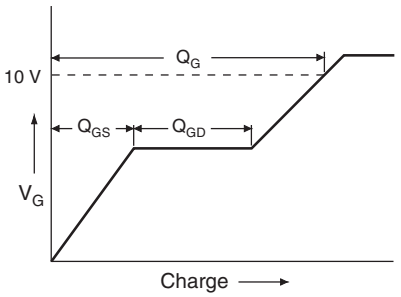


Fig. 16 - Basic Gate Charge Waveform

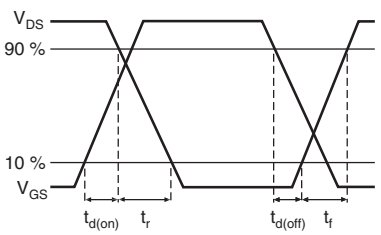


Fig. 13 - Switching Time Waveforms

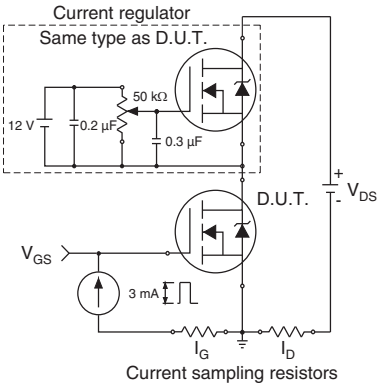


Fig. 17 - Gate Charge Test Circuit

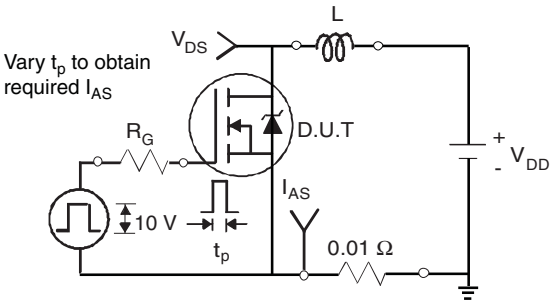


Fig. 14 - Unclamped Inductive Test Circuit

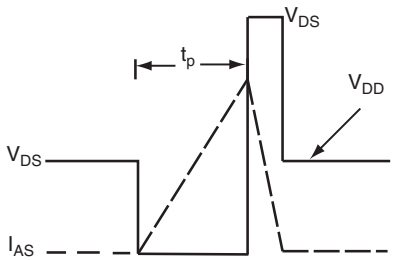
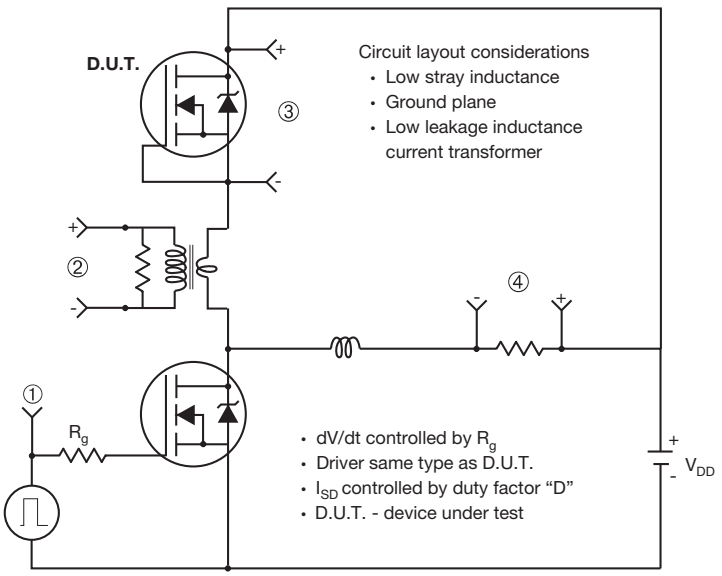
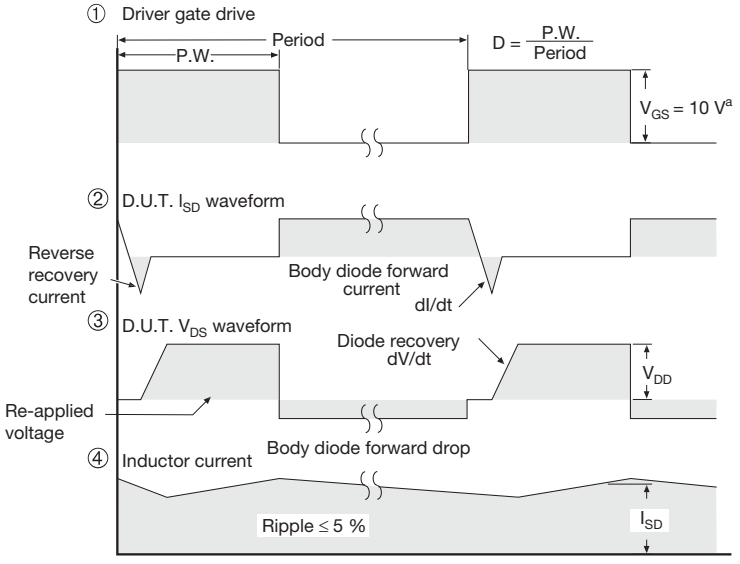


Fig. 15 - Unclamped Inductive Waveforms

Peak Diode Recovery dV/dt Test Circuit



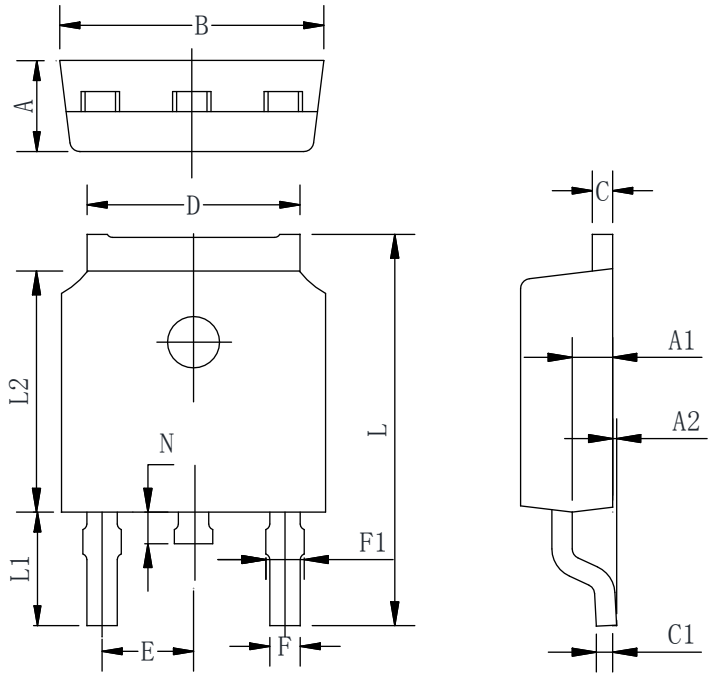


Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

TO-252-2L PACKAGE OUTLINE



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

Symbol	Min	Typ	Max
A	2.10	2.30	2.50
A1	0.88	1.01	1.16
A2	0.00	0.15	0.28
B	6.40	6.60	6.80
C	0.42	0.50	0.63
C1	0.42	0.50	0.63
D	5.08	5.32	5.65
E		2.286 TYP	
F	0.63	0.76	0.89
F1	0.64	0.86	1.08
L	9.30	9.90	10.80
L1	2.4	2.8	3.6
L2	5.90	6.10	6.55
N	0.57	0.80	1.05

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